



335 Pioneer Way  
Mt View, California 94041  
(650) 526-1490 Fax (650) 526-1494  
e-mail: sales@netchip.com  
Internet: www.netchip.com

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# NET1031 USB Scanner Controller PRELIMINARY SPECIFICATION

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## ADVANCE INFORMATION

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## Revision History

| Revision | Issue Date       | Comments  |
|----------|------------------|---|
| 0.1      | October 17, 1997 | NET1031 Initial Draft Specification Proposal                        |
| 0.2      | March 30, 1998   | 16-Bit Register initial draft                                       |
| 0.3      | July 22, 1998    | Move Applications information to AppNote.<br>Update Register layout |
| 0.4      | July 23, 1998    | Re-organize the endpoint structure                                  |
| 0.5      | Aug 27, 1998     | Re-organize registers; add new SRAM and initialization features     |
| 0.6      | Sept 11, 1998    | Add some new registers  |
| 0.7      | Oct 7, 1998      | Add some more new registers   |
| 0.8      | Nov 9, 1998      | Clarify some text. Modify some registers                            |
| 0.9      | Jan 4, 1999      | Modify some registers   |
| 0.10     | Jan 8, 1999      | Change pinouts, modify some defaults                                |
| 0.11     | Jan 17, 1999     | Modify some defaults  |
| 1.0      | Mar 19, 1999     | Modify some defaults, remove references to PRNU and B/W threshold   |

# NET1031 USB Scanner Controller

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# 1 Highlights

## 1.1 Introduction

The NetChip USB scanner engine provides a single chip solution providing a USB core and scanner imaging control in a single chip. No external microprocessor is needed in the scanner. The NET1031 replaces multiple ICs in a typical scanner design, and is fully programmable to ensure support with a wide range of scanning hardware. The NET1031 provides the necessary signaling for both color and gray scale charge-coupled devices (CCD) or contact image sensors (CIS), and contains a fully-functional USB core to control the scanner and perform image transfers across USB.

## 1.2 Features

### 1.2.1 General Features

- Single-Chip USB Scanner Controller Solution
- Low Power CMOS in 144-pin PQFP Package
- Core operates at 3.3V, dual-voltage (3.3V/5.0V) Scanner-Side Interface
- Supports 500  $\mu$ A suspend current requirement of USB
- 6 MHz crystal oscillator with internal PLL.
- Generic I/O-Space Read and Write Access for programmable external components

### 1.2.2 Scanner Features

- Supports CIS and CCD Sensors in Hardware
- Stepper Motor Controller Interface
- Up to 2 MB SRAM Interface for Image Data Buffer
- Up to 36-bit Color, 12-bit Grayscale

### 1.2.3 USB Features

- USB Specification Version 1.1 Compliant
- Supports Full-Speed USB Bandwidth of 12 Mbps
- Status Reporting through USB Interrupt Endpoint

## 1.3 Overview

The NetChip NET1031 USB scanner engine is designed to work with most CCDs and CISs. Sensor, analog acquisition subsystem, and stepper motor control signals are provided directly from the NET1031. The NET1031 is designed to work both in a pull model (such as TWAIN) and a push model. It can signal to a host driver to initiate a scan when a target has been loaded and is ready to be scanned in. The NET1031 will enter a low-power suspend mode when required by the USB, and can wake up in response to activity on either the host or the scanner. The NET1031 can also perform a “device remote wake-up” (as defined by the USB specification) to wake a host that has suspended its USB.

The NET1031 can address up to 2 Mbytes of external SRAM. This memory is used as a FIFO for a partially scanned image prior to sending it to the host. The NET1031 can be programmed to slow the scan rate to one-half speed, and stop if the FIFO becomes nearly full. This may occur when the data rate from the scanner to the host slows due to other devices on the USB or other limitations of the host.

The NET1031 interfaces directly to a stepper motor driver. Once programmed it will send the appropriate signals to energize the various coils and step the motor forward or backward.

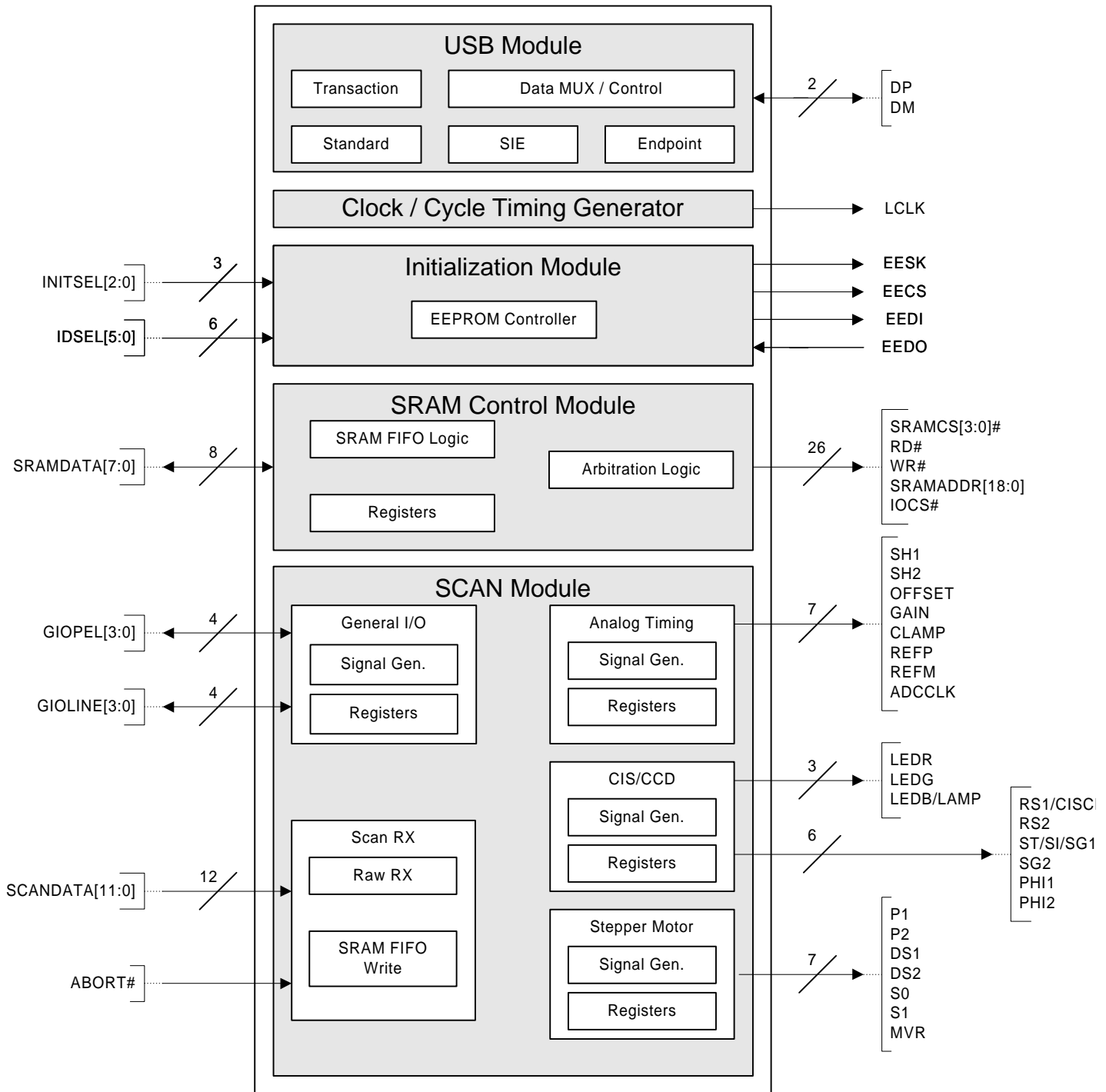
An interface to an optional external serial memory device is provided to initialize the NET1031 with parameters necessary for enumeration of the device. Parameters loaded from the serial device include the Vendor ID, Product ID, Revision Number, Maximum Power fields, and USB control bits, as well as optional string descriptors.

The NET1031 has 8 programmable general input/output pins. These signals may be configured as digital inputs, Pulse-Width Modulation (PWM) outputs, or digital outputs. The outputs themselves may be configured totem-pole or open-drain. The chip can be driven with a 6 MHz crystal or clock oscillator.

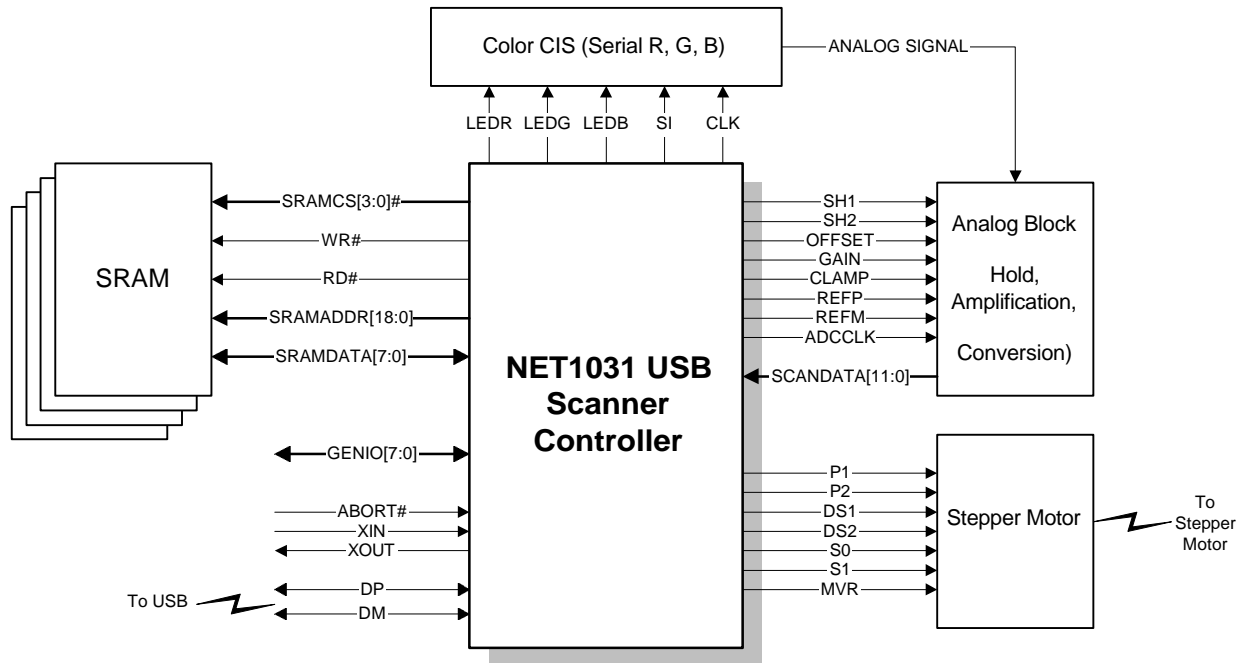


1.4 NET1031 Block Diagram

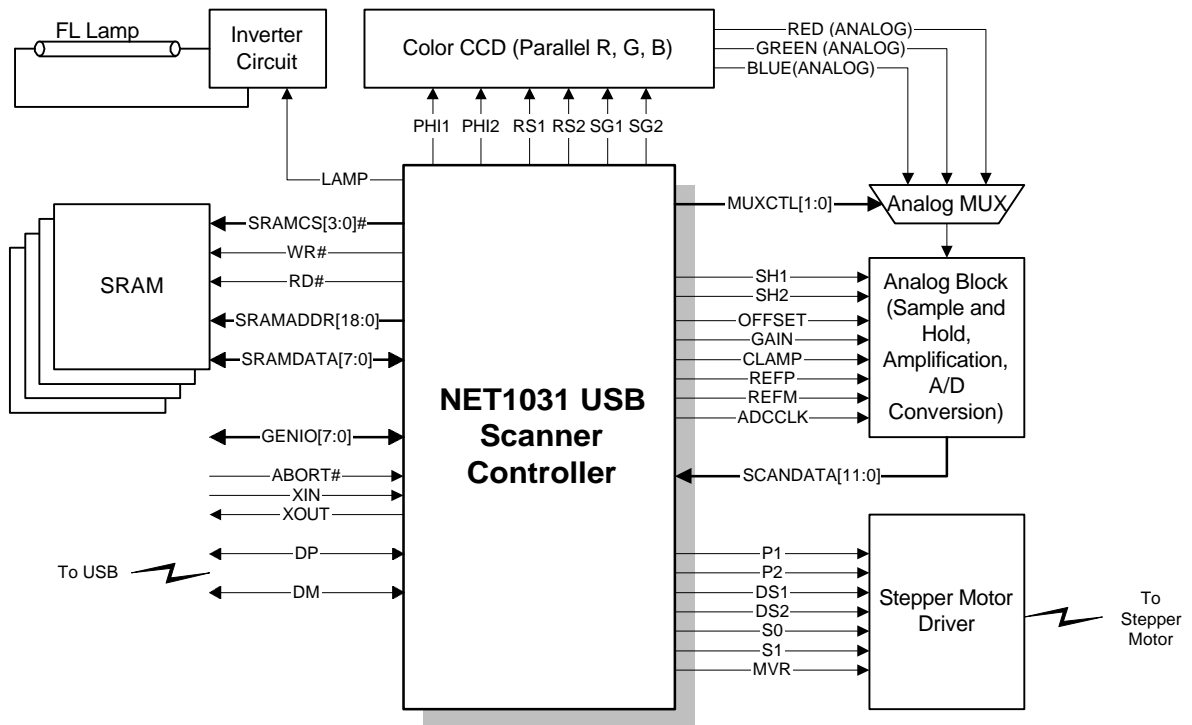
Figure 1-1: NET1031 Block Diagram



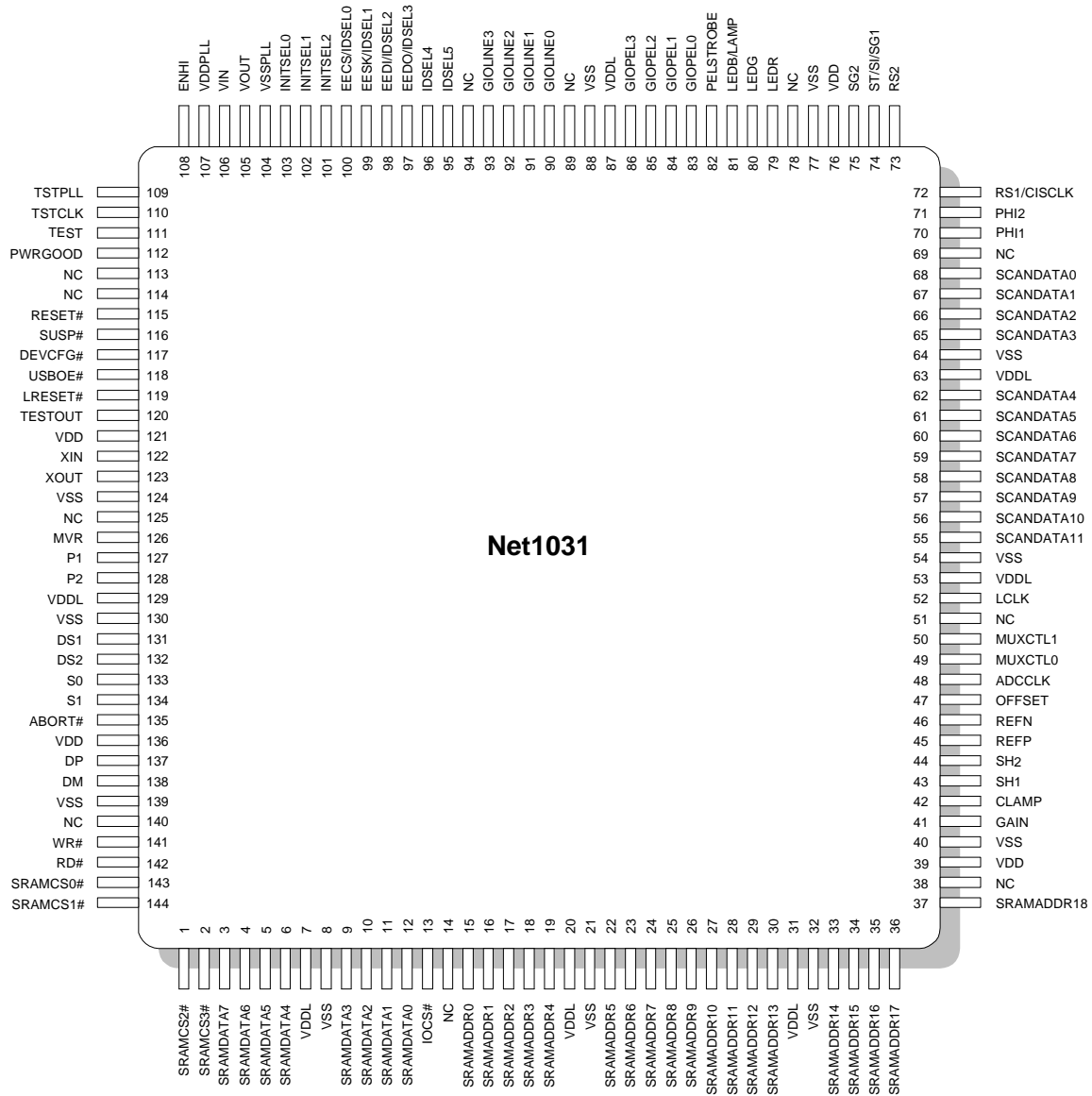
**1.5 NET1031 CIS Scanner System Block Diagram**



**1.6 NET1031 CCD Scanner System Block Diagram**



## 2 Pin Connection Diagram



### 3 Pin Description

**NOTE:** “Pin Numbers” are just being assigned sequentially to get a pin count for now.

**Table 3-1: Pin Types**

| Pin Type | Description                              |
|----------|--|
| I        | Input                                    |
| O        | Output                                   |
| I/O      | Bi-Directional (with Tri-State)          |
| S        | Schmitt Trigger                          |
| TS       | Tri-State                                |
| TP       | Totem Pole                               |
| OD       | Open Drain                               |
| PD       | 50K $\Omega$ Internal Pull-Down Resistor |
| PU       | 50K $\Omega$ Internal Pull-Up Resistor   |
| #        | Active Low                               |

**NOTE:** When the NET1031 is in the suspended state, input pins that do not have an internal pull-up or pull-down resistor (designated by PU or PD in the “Type” column) must be driven externally.

**Table 3-2: Pin Descriptions**

| Signal Name | Pin | Type           | Description  |
|-------------|-----|----------------|--|
| SCANDATA0   | 68  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA1   | 67  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA2   | 66  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA3   | 65  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA4   | 62  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA5   | 61  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA6   | 60  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA7   | 59  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA8   | 58  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA9   | 57  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA10  | 56  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| SCANDATA11  | 55  | I/O, 6mA, PU   | <b>Scan Data Bit.</b> Scan Data Input from A/D; Data Output for I/O writes |
| MUXCTL0     | 49  | O, 6mA, TS, PD | <b>MUX Control Bit.</b> Analog scan data input MUX selector                |
| MUXCTL1     | 50  | O, 6mA, TS, PD | <b>MUX Control Bit.</b> Analog scan data input MUX selector                |

|              |     |                 |  |
|--------------|-----|-----------------|--|
| ADCCLK       | 48  | O, 6mA, TS, PD  | <b>A/D Clock.</b> Provides the analog-to-digital converter clock   |
| CLAMP        | 42  | O, 6mA, TS, PD  | <b>Programmable Clamp.</b> Provides a Programmable Clamping Signal   |
| SH1          | 43  | O, 6mA, TS, PD  | <b>Sample/Hold 1.</b> Programmable Sample and Hold Signal  |
| SH2          | 44  | O, 6mA, TS, PD  | <b>Sample/Hold 2.</b> Programmable Sample and Hold Signal  |
| REFP         | 45  | O, 6mA, TS, PD  | <b>A/D Positive Ref.</b> Adjustable PWM Ref + for the A/D  |
| REFN         | 46  | O, 6mA, TS, PD  | <b>A/D Negative Ref.</b> Adjustable PWM Ref – for the A/D  |
| OFFSET       | 47  | O, 6mA, TS, PD  | <b>A/D Offset.</b> Adjustable PWM offset control   |
| GAIN         | 41  | O, 6mA, TS, PD  | <b>A/D Gain.</b> Adjustable PWM gain control   |
| PHI1         | 70  | O, 6mA, TS, PD  | <b>CCD Clock Phase 1.</b> Output Phase 1 Clock for CCD usage   |
| PHI2         | 71  | O, 6mA, TS, PD  | <b>CCD Clock Phase 2.</b> Output Phase 2 Clock for CCD usage   |
| RS1 / CISCLK | 72  | O, 6mA, TS, PD  | <b>Reset 1 Clock.</b> Output Reset 1 Clock for CCD or Clk for CIS  |
| RS2          | 73  | O, 6mA, TS, PD  | <b>Reset 2 Clock.</b> Output Reset 2 Clock for CCD   |
| ST/SI/SG1    | 74  | O, 6mA, TS, PD  | <b>Shift Gate 1.</b> Output Shift Gate Signal or end of line Clk   |
| SG2          | 75  | O, 6mA, TS, PD  | <b>Shift Gate 2.</b> Output Shift Gate 2 Signal  |
| LEDR         | 79  | O, 6mA, TS, PD  | <b>Red LED Control.</b> Output Signal to control the Red Led   |
| LEDG         | 80  | O, 6mA, TS, PD  | <b>Green LED Control.</b> Output Signal to control the Green Led   |
| LEDB / LAMP  | 81  | O, 6mA, TS, PD  | <b>Blue LED Control.</b> Output Signal to control the Blue Led or Lamp                                       |
| PELSTROBE    | 82  | O, 6mA, TS, PD  | <b>Pixel Strobe.</b> This output pulses after each pixel cycle. Rising edge captures pixel data for NET1031. |
| GIOPEL0      | 83  | I/O, 12mA, PU   | <b>General Pixel-based I/O bit.</b> Programmable I/O, PWM or Digital.  |
| GIOPEL1      | 84  | I/O, 12mA, PU   | <b>General Pixel-based I/O bit.</b> Programmable I/O, PWM or Digital   |
| GIOPEL2      | 85  | I/O, 12mA, PU   | <b>General Pixel-based I/O bit.</b> Programmable I/O, PWM or Digital   |
| GIOPEL3      | 86  | I/O, 12mA, PU   | <b>General Pixel-based I/O bit.</b> Programmable I/O, PWM or Digital   |
| GIOLINE0     | 90  | I/O, 12mA, PU   | <b>General Line-based I/O bit.</b> Programmable I/O, PWM or Digital  |
| GIOLINE1     | 91  | I/O, 12mA, PU   | <b>General Line-based I/O bit.</b> Programmable I/O, PWM or Digital  |
| GIOLINE2     | 92  | I/O, 12mA, PU   | <b>General Line-based I/O bit.</b> Programmable I/O, PWM or Digital  |
| GIOLINE3     | 93  | I/O, 12mA, PU   | <b>General Line-based I/O bit.</b> Programmable I/O, PWM or Digital  |
| ABORT#       | 135 | I, PU           | <b>Abort Scan.</b> Abort Scan control  |
| WR#          | 141 | O, 12mA, TS, PU | <b>Write Strobe.</b> Write strobe for external SRAM and I/O writes   |
| RD#          | 142 | O, 12mA, TS, PU | <b>Read Strobe.</b> Read strobe for external SRAM and I/O reads  |
| SRAMCS0#     | 143 | O, 6mA, TS, PU  | <b>SRAM Chip Select.</b> Chip Select 0 for the external SRAM   |
| SRAMCS1#     | 144 | O, 6mA, TS, PU  | <b>SRAM Chip Select.</b> Chip Select 1 for the external SRAM   |
| SRAMCS2#     | 1   | O, 6mA, TS, PU  | <b>SRAM Chip Select.</b> Chip Select 2 for the external SRAM   |
| SRAMCS3#     | 2   | O, 6mA, TS, PU  | <b>SRAM Chip Select.</b> Chip Select 3 for the external SRAM   |
| IOCS#        | 13  | O, 6mA, TS, PU  | <b>I/O Chip Select.</b> Chip select for external I/O cycles.   |

|            |    |                 |   |
|------------|----|-----------------|---|
| SRAMADDR0  | 15 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR1  | 16 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR2  | 17 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR3  | 18 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR4  | 19 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR5  | 22 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR6  | 23 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR7  | 24 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR8  | 25 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR9  | 26 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR10 | 27 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR11 | 28 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR12 | 29 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR13 | 30 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR14 | 33 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM or I/O device |
| SRAMADDR15 | 34 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM               |
| SRAMADDR16 | 35 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM               |
| SRAMADDR17 | 36 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM               |
| SRAMADDR18 | 37 | O, 12mA, TS, PU | <b>SRAM Address Bus Bit.</b> Address Bus to external image SRAM               |
| SRAMDATA0  | 12 | I/O, 12mA, PU   | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device      |
| SRAMDATA1  | 11 | I/O, 12mA, PU   | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device      |
| SRAMDATA2  | 10 | I/O, 12mA, PU   | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device      |
| SRAMDATA3  | 9  | I/O, 12mA, PU   | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device      |
| SRAMDATA4  | 6  | I/O, 12mA, PU   | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device      |

|              |  |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
|--------------|--|----------------|--|-----|--|--------------|--------|-------|--------------------------------------|-------|--------------------------------------|-------|--------------------|-------|--------------------|-------|--|-------|----------|-------|----------|-------|--------------------|
| SRAMDATA5    | 5  | I/O, 12mA, PU  | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| SRAMDATA6    | 4  | I/O, 12mA, PU  | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| SRAMDATA7    | 3  | I/O, 12mA, PU  | <b>SRAM Data Bus Bit.</b> Data Bus to / from external SRAM or I/O device   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| MVR          | 126  | O, 6mA, TS, PD | <b>Throttle.</b> Stepper motor throttle control  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| P1           | 127  | O, 6mA, TS, PD | <b>Energize Phase 1.</b> Energize Phase 1 of Stepper Motor   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| P2           | 128  | O, 6mA, TS, PD | <b>Energize Phase 2.</b> Energize Phase 2 of Stepper Motor   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| DS1          | 131  | O, 6mA, TS, PU | <b>Disable Phase 1.</b> Disable Phase 1 of Stepper Motor   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| DS2          | 132  | O, 6mA, TS, PU | <b>Disable Phase 2.</b> Disable Phase 2 of Stepper Motor   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| S0           | 133  | O, 6mA, TS, PD | <b>Voltage Reference Selector.</b> Select one of four voltage references for Stepper Motor.  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| S1           | 134  | O, 6mA, TS, PD | <b>Voltage Reference Selector.</b> Select one of four voltage references for Stepper Motor.  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| INITSEL0     | 103  | I, PU          | <b>Initialization Select Bit 0.</b> Select source of register initialization data.   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| INITSEL1     | 102  | I, PU          | <b>Initialization Select Bit 1.</b> Select source of register initialization data.   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| INITSEL2     | 101  | I, PU          | <b>Initialization Select Bit 2.</b> Select source of register initialization data.<br><table border="0"> <tr> <td>Bit</td> <td></td> </tr> <tr> <td><u>2 1 0</u></td> <td>Source</td> </tr> <tr> <td>0 0 0</td> <td>E<sup>2</sup>PROM (93CS46, 93CS06)</td> </tr> <tr> <td>0 0 1</td> <td>E<sup>2</sup>PROM (93CS56, 93CS66)</td> </tr> <tr> <td>0 1 0</td> <td>Serial ROM 1 (TBD)</td> </tr> <tr> <td>0 1 1</td> <td>Serial ROM 2 (TBD)</td> </tr> <tr> <td>1 0 0</td> <td>IDSEL pins determine lower 6 bits of Product ID.</td> </tr> <tr> <td>1 0 1</td> <td>Reserved</td> </tr> <tr> <td>1 1 0</td> <td>Reserved</td> </tr> <tr> <td>1 1 1</td> <td>Use default values</td> </tr> </table> | Bit |  | <u>2 1 0</u> | Source | 0 0 0 | E <sup>2</sup> PROM (93CS46, 93CS06) | 0 0 1 | E <sup>2</sup> PROM (93CS56, 93CS66) | 0 1 0 | Serial ROM 1 (TBD) | 0 1 1 | Serial ROM 2 (TBD) | 1 0 0 | IDSEL pins determine lower 6 bits of Product ID. | 1 0 1 | Reserved | 1 1 0 | Reserved | 1 1 1 | Use default values |
| Bit          |  |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| <u>2 1 0</u> | Source   |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 0 0 0        | E <sup>2</sup> PROM (93CS46, 93CS06)             |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 0 0 1        | E <sup>2</sup> PROM (93CS56, 93CS66)             |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 0 1 0        | Serial ROM 1 (TBD)                               |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 0 1 1        | Serial ROM 2 (TBD)                               |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 1 0 0        | IDSEL pins determine lower 6 bits of Product ID. |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 1 0 1        | Reserved   |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 1 1 0        | Reserved   |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| 1 1 1        | Use default values                               |                |  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| EECS/IDSEL0  | 100  | I/O, 6mA, PD   | <b>E<sup>2</sup>PROM Chip Select/ID Select bit 0.</b>  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| EESK/IDSEL1  | 99   | I/O, 6mA, PD   | <b>E<sup>2</sup>PROM Clock/ID Select bit 1.</b>  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| EEDI/IDSEL2  | 98   | I/O, 6mA, PD   | <b>E<sup>2</sup>PROM Write Data/ID Select bit 2.</b>   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| EEDO/IDSEL3  | 97   | I, PU          | <b>E<sup>2</sup>PROM Read Data/ID Select bit 3.</b>  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| IDSEL4       | 96   | I, PU          | <b>ID Select bit 4.</b>  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| IDSEL5       | 95   | I, PU          | <b>ID Select bit 5.</b>  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| RESET#       | 115  | I, S, PU       | <b>Reset.</b> Connect to local or power-on reset. To reset when the oscillator is stopped (initial power-up or in suspend state), assert for at least 2 ms. When oscillator is running, assert for at least five 48-MHz clock periods.   |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |
| LRESET#      | 119  | O, 6mA, TS, PU | <b>Local Reset.</b> This active low output is asserted when either the RESET# pin is asserted, or a USB upstream port reset is detected. This signal is not driven while the device is suspended, but will be pulled high by the internal pull-up resistor.  |     |  |              |        |       |                                      |       |                                      |       |                    |       |                    |       |  |       |          |       |          |       |                    |

|                   |                                  |                |  |
|-------------------|----------------------------------|----------------|--|
| DM                | 138                              | I/O            | <b>USB Data Port.</b> DP and DM are differential data signals of the USB data port.  |
| DP                | 137                              | I/O            | <b>USB Data Port.</b> DP and DM are differential data signals of the USB data port. An external 1.5 K $\Omega$ resistor must be connected from DP to +3.3V. This pull-up resistor indicates to the host or upstream hub that a full-speed device is connected to the USB.  |
| DEVCFG#           | 117                              | O, 6mA, TS, PD | <b>Device Configured.</b> This active low output is true when the USB host has configured the NET1031. This bit is initialized to inactive (high) during reset and is set true when the host issues a Set Configuration request. This signal is not driven while the device is suspended, but will be pulled low by the internal pull-down resistor. |
| USBOE#            | 118                              | O, 6mA, TS, PU | <b>USB Port Output Enable.</b> This is an active low output that is asserted when the NET1031 is driving the USB port data lines. This signal is not driven while the device is suspended, but will be pulled high by the internal pull-up resistor.   |
| PWRGOOD           | 112                              | I, S, PD       | <b>Power Good.</b> This active high input indicates that an external power supply used for self-powered mode is operational.   |
| SUSP#             | 116                              | O, 6mA, TS, PD | <b>Device Suspended.</b> This active low output is true when the USB host has suspended the NET1031. This signal is not driven while the device is suspended, but will be pulled low by the internal pull-down resistor.   |
| LCLK              | 52                               | O, 6mA, TS, PD | <b>Local Clock.</b> This clock is derived from the 6-MHz crystal or oscillator connected to CLKIN. This signal is not driven while the device is suspended, but will be pulled low by the internal pull-down resistor. The USB Control Register selects the frequency of this pin (0, 6, 12, 24, 48 MHz).  |
| TESTOUT           | 120                              | O              | <b>Test Output.</b> Leave as No Connect  |
| TEST              | 111                              | I, PD          | <b>Test Mode.</b> Set to 0 for normal operation.   |
| XIN               | 122                              | I              | <b>6 MHz Oscillator Input.</b> Connect to 6 MHz crystal or external oscillator module.   |
| XOUT              | 123                              | O              | <b>6 MHz Oscillator Output.</b> Connect to 6 MHz crystal, or leave unconnected if using an external oscillator module. The oscillator stops when the USB Host suspends the device.   |
| TSTCLK            | 110                              | I, PD          | <b>PLL Test Clock.</b> Clock input for PLL testing. Set to 0 or leave as no connect.   |
| TSTPLL            | 109                              | I, PD          | <b>PLL Test Enable.</b> Set to 0 or leave as no connect.   |
| ENHI              | 108                              | I, PU          | <b>PLL Enable.</b> Set to 0 to bypass the PLL. In this case, an external 48 MHz signal must be applied to the XIN input.   |
| VDDPLL            | 107                              | Pwr            | <b>PLL Supply Voltage.</b> VDDPLL = 3.3V   |
| VSSPLL            | 104                              | Gnd            | <b>PLL Supply Voltage.</b> VSSPLL = GND  |
| VIN               | 106                              | I              | <b>PLL Filter Input</b> Connect to VOUT with an RC (46K $\Omega$ , 64pF) to ground.  |
| VOUT              | 105                              | O              | <b>PLL Filter Output</b>   |
| VDD<br>(VDDCORE)  | 39, 76, 121,<br>136              | Pwr            | <b>Core Supply Voltage.</b> VDD = 3.3V   |
| VDDL<br>(VDDSCAN) | 7, 20, 31,<br>53, 63, 87,<br>129 | Pwr            | <b>Scanner-side Supply Voltage.</b> Dual voltage, VDDL = 3.3V or 5.0V  |



|     |   |     |   |
|-----|---|-----|---|
| VSS | 8, 21, 32,<br>40, 54, 64,<br>77, 88, 124,<br>130, 139       | Gnd | <b>Device Ground.</b>                         |
| NC  | 14, 38, 51,<br>69, 78, 89,<br>94, 113,<br>114, 125,<br>140, |     | <b>No Connect.</b> Do not connect these pins. |

Note: All TS and I/O pins are tri-stated during the Suspend state.

## 4 Functional Description

### 4.1 Start-Up

Before the NET1031 is ready to perform scanning functions, a sequence of operations must occur, involving the NET1031, the USB driver stack, and the host Scanner driver. First, the NET1031 reads required USB parameters from the external serial memory device. Next, the USB driver stack must enumerate the NET1031. Finally the host scanner driver configures the NET1031 with the correct parameters for the scanner.

#### 4.1.1 Reading from Initialization Device

When the NET1031 first comes out of a reset applied at its RESET# input pin or provided by the USB host, it reads various parameters required by the USB host from an external serial memory. The INITSEL[2:0] pins determine the source of the initialization parameters. The NET1031 generates all signals necessary to read the data from the serial memory, so no interaction is required from the scanner hardware. Until this data is read, the NET1031 will respond to host requests for a configuration descriptor or device descriptor with a NAK. If no valid serial memory device is installed, then either the default values are used, or the lower six bits of the product ID can be modified using the IDSEL input pins. These options are selected using the INITSEL[2:0] pins.

#### 4.1.2 Enumeration by the Host PC

USB defines a set of descriptor requests and calls that are part of the enumeration process. The NET1031 responds to these requests. When enumeration is complete, the USB host will perform a “Set Configuration” request, which signals the end of the enumeration process. The NET1031’s DEVCFG# output pin will activate. At that point, control over the NET1031 is passed to the host scanner driver.

As part of the enumeration process, the USB host issues a Get Device Descriptor request, which the NET1031 answers with various parameters, including the Vendor ID and Product ID read from the external serial memory. This Vendor ID and Product ID allow the host to associate the vendor-supplied scanner driver with the NET1031.

#### 4.1.3 Configuration by the Scanner Driver

Before a scan may be performed, the host PC’s scanner driver must configure the NET1031. The registers programming the PWM signals and other parameters must be initialized. Any register for which the default values are not appropriate should be set.

#### 4.1.4 Global Calibration

An optional step is to perform Global Calibration. Global Calibration should be performed once when the scanner is plugged into a PC for the first time. Subsequent calibrations are optional, since the calibration data may be stored in the Host PC after the first time, and downloaded to the scanner on subsequent plug-ins.

## 4.2 Initialization Interface

The NET1031 can be initialized at reset time from several sources, selected by the INITSEL[2:0] bits. The initialization must be completed before the NET1031 will respond to Device Descriptor requests from the host.

| INITSEL[2:0] | Source                               |
|--------------|--------------------------------------|
| 0            | E <sup>2</sup> PROM (93CS06, 93CS46) |
| 1            | E <sup>2</sup> PROM(93CS56, 93CS66)  |
| 2            | Reserved                             |
| 3            | Reserved                             |
| 4            | IDSEL Pins                           |
| 5            | Reserved                             |
| 6            | Reserved                             |
| 7            | Default                              |

### 4.2.1 E<sup>2</sup>PROMs (93CS06, 93CS46, 93CS56, 93CS66)

The 93CS06 (32 bytes), 93CS46 (128 bytes), 93CS56 (256 bytes), or the 93CS66 (512 bytes), can be used to initialize registers in the NET1031. Each of these devices has a 4-wire MicroWire™ serial interface. After reset is negated, the INITSEL bits are sampled to determine the source of the initialization information. If INITSEL[2:0] = 0 or 1, then the NET1031 will determine if a non-blank E<sup>2</sup>PROM is connected. If no E<sup>2</sup>PROM is detected, or the device is blank (first word is FFFF), then the default register values will be reported to the Host PC. Otherwise the following required fields are loaded into the NET1031 from the E<sup>2</sup>PROM. These required fields are reported in the Device and Configuration descriptors during USB device enumeration. Information is stored in the EEPROM as 16-bit words. For string descriptors, bits 7:0 of an EEPROM word are returned to the host first, followed by bits 15:8.

**Table 4-1: Required Serial E<sup>2</sup>PROM Fields**

| Word Index    | Contents  | Default Value   |
|---------------|---|---|
| 0             | <b>Vendor ID.</b> This field is reported to the Host PC in the USB device descriptor's "Vendor ID" field during enumeration.  | 0x0525  |
| 1             | <b>Product ID.</b> This field is reported to the Host PC in the USB device descriptor's "Product ID" field during enumeration.  | 0x1031  |
| 2             | <b>Revision ID.</b> This field is reported to the Host PC in the USB device descriptor's "Revision ID" field during enumeration.  | 0xr <sub>rrr</sub> , r <sub>rrr</sub> = Silicon Rev # |
| 3             | <b>Max Power.</b> This field is reported to the Host PC in the USB configuration descriptor's "Max Power" field during enumeration. It is reported in units of 2mA. This field should reflect the maximum current drawn by the scanner from the USB power pins. | 0x0032  |
| 4             | <b>USB Features 1.</b> This field breaks down into several control bits that are reported to the Host PC in the USB device descriptor and configuration descriptor. See <b>USB Control Register 1</b> for details.  | 0x0103  |
| 5             | <b>USB Features 2.</b> This field breaks down into several control bits that are reported to the Host PC in the USB device descriptor and configuration descriptor. See <b>USB Control Register 2</b> for details.  | 0x0001  |
| 6 (bits 15:8) | <b>Language ID String Start Index.</b>  | 0x0000  |
| 6 (bits 7:0)  | <b>Manufacturer String Start Index.</b>   | 0x0000  |
| 7 (bits 15:8) | <b>Product String Start Index.</b>  | 0x0000  |
| 7 (bits 7:0)  | <b>Serial Number String Start Index.</b>  | 0x0000  |

In addition, if any “String Enable” fields are set in **USB Control Register 2**, the fields in Table 4-2 must be defined.

**Table 4-2: Additional Serial E<sup>2</sup>PROM Fields for String Descriptors**

| Word Index | Contents   |
|------------|--|
| 8-9        | <b>Reserved.</b> Write these words as a zero.  |
| 0Ah-FFh    | <b>Available.</b> This range of the serial EPROM is available for defining string descriptors. |

If no string descriptors are used, the E<sup>2</sup>PROM image may be as short as 8 words (to provide the required fields to the Host PC). With string descriptors, the E<sup>2</sup>PROM can end at the end of the last string descriptor’s definition.

The MicroWire EEPROMs can be accessed from host using the EEADDR and EEDATA registers. For an EEPROM write, the host first writes the data to the EEDATA register. Then the write is initiated by writing the EEPROM address, Read/Write bit, and Start bit to the EEADDR register. The host may then poll the Start bit until it is cleared, indicating that the write operation is complete.

An EEPROM read is initiated by writing the EEPROM address, Read/Write bit, and Start bit to the EEADDR register. The host may then poll the Start bit until it is cleared, indicating that the read operation is complete. The data is then read from the EEDATA register.

For EEPROMs that are not MicroWire compatible, the host can directly manipulate the EEPROM control signals using the EECTL register. Note that the EEPROM control signals are enabled only if the INITSEL pins are not set to 4.

#### 4.2.2 IDSEL Pin Initialization

If INITSEL[2:0] = 4, then the least significant 6 bits of the idProduct field in the device descriptor are determined by the IDSEL[5:0] pins. All other initialization values are left in the default state.

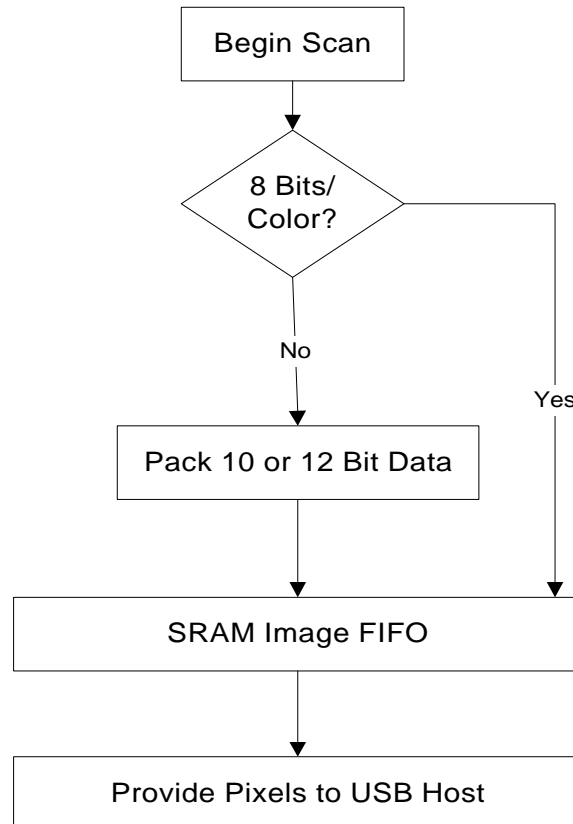
### 4.3 Scanner Functions

#### 4.3.1 CCD/CIS Control

The NET1031 can control a wide variety of CIS and CCD sensors. The CIS and CCD control signals are programmable pulse width modulated (PWM) signals. See Section 9 for a description of the PWM signals.

#### 4.3.2 General Data Flow

**Figure 4-1: General Image Data Flow**



### 4.3.3 Analog Block Interface

Analog image acquisition support signals are also generated using pulse-width modulation (PWM) techniques. PWM signals, in conjunction with an external RC circuit, provide a mechanism for generating digital control signals and analog voltages to control the analog block. Signals such as Gain and Offset can therefore be specified at analog voltage levels. See Section 9 for a description of the PWM signals.

### 4.3.4 Stepper Motor Control

The NET1031 can control a variety of stepper motors. The enable, disable, and voltage reference selector signals for two phases are present and fully programmable as PWM signals.

### 4.3.5 Image Buffering in SRAM

Image data, once it is scanned, is placed in the external SRAM by the NET1031 to be queued for transmission over USB. The SRAM allows the scanner to continue a scan in progress if a host PC temporarily slows in reading data from the NET1031. The NET1031 supports the following memory configurations:

| SRAM Type | Max Number of Rams | Total Max Memory | Buffering* |
|-----------|--------------------|------------------|------------|
| 32Kx8     | 4                  | 128K             | 116 msec   |
| 128Kx8    | 4                  | 512K             | 509 msec   |
| 512Kx8    | 4                  | 2M               | 2.08 sec   |

- Assume a typical scenario of 24 bits per pixel at a rate of 3 usec per pixel. The SRAM buffer is able to store pixel data for the time period shown in the chart, and is calculated as follows:  

$$\text{Buffering time} = (\text{Max Memory}) * (8/\text{bits per pixel}) * (\text{pixel time}) =$$

$$(83\text{K}) * (8/24) * (3\text{usec}) = 83 \text{ msec}$$
- At 36 bits per pixel, the buffering time is:  

$$\text{Buffering time} = (\text{Max Memory}) * (8/\text{bits per pixel}) * (\text{pixel time}) =$$

$$(83\text{K}) * (8/36) * (3\text{usec}) = 55 \text{ msec}$$

The SRAM buffer generally does not contain enough memory to store an entire image, so on average the Host PC must accept data at a rate greater than or equal to the scan rate. If this condition is not met, the SRAM buffer may fill. At that point, the NET1031 will have to slow and/or stop the scan operation while waiting for room to become available in the SRAM. The NET1031 can adjust the scanning speed to half speed, or stop as it approaches multiple threshold levels of memory filled in the SRAM.

### 4.3.6 General I/O Pins

The NET1031 includes 8 general input/output pins. Each of these eight pins may be independently configured as digital inputs, digital outputs, or PWM outputs. Outputs may be totem-pole or open-drain. When configured as PWM outputs, four General I/O pins (GIOLINE0-GIOLINE3) can have transitions programmed in units of scanlines, while four pins (GIOPEL0-GIOPEL3) can have transitions programmed in units of pixel timing. When configured as inputs, the value of the eight pins may be read from the General I/O registers. Some potential uses of these pins are:

- Paper Out: input asserted when a sheet of paper has moved out of the scanner (from auto-feed system).
- Paper In: input asserted when a sheet of paper is in the scanner.
- Restore Sensor: input asserted when the scanhead of a flatbed scanner has restored to the home position.
- Page Feed: output to cause an auto-feeder to feed the next page into the scanner.
- Serial A/D Controls: outputs that allow analog-to-digital converter control registers to be written using a serial protocol.
- Start Scan: In a push model, this input from a front panel pushbutton could cause a scanning application to start.

- Front Panel LED: Output to cause an LED to be illuminated when USB communications are established.

#### 4.3.7 Abort# Pin

When this active low input is asserted, a status bit is set which indicates to the host that it should stop the scan. Also, the **Enable Stepper** and **Enable Pixel Processing** bits in the MASTERCTL register are cleared. When **Enable Stepper** is cleared, the stepper control output pins are returned to their default state.

### 4.4 USB Interface

The interface from the NET1031 to USB allows the Host PC to accept scanned data, access registers, read and write SRAM data, perform I/O operations, and control the scanner operation.

#### 4.4.1 Default Control Pipe (Endpoint 0x00)

Endpoint 0 is a bi-directional USB control endpoint which processes 8-byte packets to/from the Host PC. Each packet is decoded and USB control read and write 'requests' are handled automatically. Endpoint 0 supports the required USB protocol read and write requests (e.g. descriptor reads), as well as vendor-specific extensions. The vendor-specific extensions provide the capability to read and write registers and perform external I/O read and write operations.

#### 4.4.2 SRAM Write Pipe (Endpoint 0x01)

Endpoint 0x01 is a USB bulk OUT endpoint that accepts packets up to 64 bytes in length. The SRAM Write Endpoint will write data received to this endpoint to the SRAM beginning at the address specified by the **SRAMADDR** register. The **SRAMADDR** register is auto-incremented as the data is written.

#### 4.4.3 SRAM/Image Data Read Pipe (Endpoint 0x81)

Endpoint 0x81 is a USB bulk IN endpoint which will transmit packets of 64 bytes. A bit in the MASTERCTL configuration register, EP81 Mode, determines the source of data for this endpoint. When the EP81 Mode bit is low, this endpoint responds to an IN token with scanned image data from the external SRAM FIFO, as it becomes available. When the EP81 Mode bit is high, this endpoint responds to an IN token with 64 bytes of SRAM data, beginning at the address specified by the **SRAMADDR** register. The **SRAMADDR** register is auto-incremented as the data is read.

#### 4.4.4 Status Input Pipe (Endpoint 0x82)

Endpoint 0x82 is a USB interrupt IN endpoint that transmits status information each time it is polled by the USB host. The transmitted information is:

- Byte 0 : SCANCHG register (LSB)
- Byte 1 : SCANCHG register (MSB)
- Byte 2 : IOCHG register (LSB)
- Byte 3 : IOCHG register (MSB)

## 4.5 I/O Space Access

To support external programmable components, the NET1031 can write and read data by providing generic I/O bus signaling. RD# and WR# strobes are also provided, as well as an IOCS# signal to indicate that we are currently operating in I/O space. When the Host PC issues a request to write to an I/O address, the NET1031 issues a 15-bit address from the SRAMADDR[14:0] pins. Bit 15 of the address is used to select between internal register accesses and external I/O accesses. If **IO Space Data Bus Select** in the MEMIOCTL register is low, the upper 12 bits of data are driven out on the SCANDATA[11:0] pins. If the **IO Space Data Bus Select** is high, the lower bits of data are driven out on the SRAMDATA[7:0] pins. For read cycles, if **IO Space Data Bus Select** is low, the data is read in from the SCANDATA[11:0] pins and returned in the most significant 12 bits. If **IO Space Data Bus Select** is high, the data is read in from the SRAMDATA[7:0] pins and returned in the least significant 8 bits.

## 4.6 Suspend Mode

When there is a three-millisecond period of inactivity on the USB, the USB specification requires a device to enter into a low-power suspended state. While in this state the device may not draw more than 500  $\mu$ A of current from the USB connector's power pins. To facilitate this, the NET1031 automatically enters the suspend state after detecting the three millisecond period of inactivity. Additionally, the NET1031 allows local bus hardware to initiate a "device remote wake-up" to the USB. When a suspend state is detected, a scan in progress will be aborted at the end of the current line.

### 4.6.1 The Suspend Sequence

The typical sequence of a suspend operation is as follows:

- During device configuration, a bit is set in the USB Control register which enables the suspend feature. (Devices which are self-powered may not need the NET1031 to enter the suspend state)
- When the USB is idle for three milliseconds, the NET1031 enters the suspend state, if enabled.

In the suspended state, the NET1031's oscillator shuts down, and most output pins are tri-stated to conserve power (see section 3, **Pin Description**). As the NET1031 enters the suspend state, the SUSP# output pin will be driven low for 20 nsec and then floated. It has an internal pull-down resistor to keep it low during suspend. Note that input pins on the NET1031 which do not have an internal pull-up or pull-down resistors should not be allowed to float during suspend mode. The NET1031 will leave suspend mode by detecting a host initiated wake-up or by a device remote wake-up.

### 4.6.2 Host-Initiated Wake-Up

The host may wake up the NET1031 by driving any non-idle state on the USB. The NET1031 will detect the host's wake-up request, and re-starts its internal oscillator. Two milliseconds later, the SUSP# output signal is driven high to indicate that the NET1031 has completed its wake-up.

### 4.6.3 Device-Remote Wake-Up

The device hardware signals a device remote wake-up by driving one of the GIOPEL or GIOLINE pins to the active state. The GIO pin and polarity are set in the USB Control Register. If the **Device Remote Wake-up Enable** bit is set, the NET1031 will send a 10-ms wake-up signal to the USB host, and concurrently re-start its local oscillator. Two milliseconds after the wakeup pin is asserted, the SUSP# line is driven high to indicate that the NET1031 has completed its wake-up.



#### 4.7 Root Port Reset

If the SIE in the NET1031 detects a single-ended zero on the root port for greater than 2.5 microseconds, it is interpreted as a root port reset. The LRESET# output pin is asserted, and the following resources are reset:

- SIE
- USB state machines
- Scanner state machines
- **Device Configured** output pin, DEVCFG#
- All configuration registers

#### 4.8 NET1031 Power Configuration

The USB specification defines both bus-powered and self-powered devices. A *bus-powered* device is a peripheral that derives all of its power from the upstream USB connector, while a *self-powered* device has an external power supply. The NET1031 is well suited for both types of applications.

The most significant consideration when deciding whether to build a bus-powered or a self-powered device is power consumption. The USB specification specifies the following requirements for maximum current draw:

- A peripheral not configured by the host may draw only 100 mA from the USB power pins.
- A device may not draw more than 500 mA from the USB connector's power pins.
- In suspend mode, the peripheral may not draw more than 500  $\mu$ A from the USB connector's power pins

If these power considerations can be met without the use of an external power supply, the peripheral can be bus-powered; otherwise a self-powered design should be implemented.

##### 4.8.1 Bus-Powered Device

If the scanner signals are powered at 3.3 Volts, the  $V_{DD}$  and  $V_{DDL}$  pins of the device are connected to a 3.3 Volt regulated source derived from the USB 5.0 volt power pin. For 5.0 volt scanner signals, the  $V_{DDL}$  pin may be connected directly to the USB 5.0 Volt power pin, while the  $V_{DD}$  pins must still be connected to 3.3 Volts through a regulator. The rest of the scanner-side circuitry is also connected to the USB power pin, either through a regulator or directly. Therefore, the peripheral's scanner circuitry and the NET1031 will all power up simultaneously, and initialization can occur normally with a power-on reset.

##### 4.8.2 Self-Powered Device

Generally, a peripheral with higher power requirements will be self-powered. In a self-powered device, the NET1031  $V_{DD}$  and  $V_{DDL}$  pins are powered by the device power supply. The USB connector's power pin is connected only to the 1.5 K $\Omega$  pull-up resistor on DP.

## 5 Register Descriptions

The NET1031 contains a 256 x 16-bit local register space that can be accessed by the Host over USB using Endpoint 0. When the NET1031 receives a RESET signal from the RESET# pin or from a USB RESET command, the registers are set to their default values.

Writes to reserved registers are ignored, and reads from reserved registers return a value of 0. For compatibility with future revisions, unused bits within a register should always be written with a zero.

Registers are organized in the address space according to function, as shown below:

| Address Range | Register Set            | Register Set Description                                       |
|---------------|-------------------------|--|
| 00 h - 2F h   | Control                 | Control, Configuration, and Status Registers.                  |
| 30 h - 3F h   | (Reserved)              | Reserved for future use  |
| 40 h - 8F h   | Pixel-based waveforms   | Configuration registers for pixel-based programmable signals   |
| 90 h - CF h   | Line-based waveforms    | Configuration registers for line-based programmable signals    |
| D0 h - EF h   | Stepper-based waveforms | Configuration registers for stepper-based programmable signals |
| F0 h - FF h   | USB                     | USB Descriptor registers                                       |

## 5.1 Control Registers Description

### 5.1.1 Control Registers Summary

| Address     | Register Name | Register Description           |
|-------------|---------------|--------------------------------|
| 00 h        | MASTERCTL     | Master Control                 |
| 01 h        | MEMIOCTL      | Memory, I/O Control            |
| 02 h        | PIXCTL        | Pixel Control                  |
| 03 h        | IOCFG         | I/O Pin Configuration          |
| 04 h        | SCANSTAT      | Scanner Status                 |
| 05 h        | IOSTAT        | I/O Pin Status                 |
| 06 h        | SCANCHG       | Scanner Status Change          |
| 07 h        | IOCHG         | I/O Pin Status Change          |
| 08 h        | SRAMADDR1     | SRAM Address, MSW              |
| 09 h        | SRAMADDR0     | SRAM Address, LSW              |
| 0A h - 0F h | (Reserved)    |                                |
| 10 h        | SRAMBASE1     | SRAM FIFO Base Address, MSW    |
| 11 h        | SRAMBASE0     | SRAM FIFO Base Address, LSW    |
| 12 h        | SRAMTOP1      | SRAM FIFO Top Address, MSW     |
| 13 h        | SRAMTOP0      | SRAM FIFO Top Address, LSW     |
| 14 h        | FIFOFSTHR1    | FIFO Full-Speed Threshold, MSW |
| 15 h        | FIFOFSTHR0    | FIFO Full-Speed Threshold, LSW |
| 16 h        | FIFOHSTHR1    | FIFO Half-Speed Threshold, MSW |
| 17 h        | FIFOHSTHR0    | FIFO Half-Speed Threshold, LSW |
| 18 h        | FIFOSTOPTHR1  | FIFO Stop Threshold, MSW       |
| 19 h        | FIFOSTOPTHR0  | FIFO Stop Threshold, LSW       |
| 1A h        | FIFOCOUNT1    | FIFO Byte Count, MSW           |
| 1B h        | FIFOCOUNT0    | FIFO Byte Count, LSW           |
| 1C h        | FIFOSTAT      | FIFO Status                    |
| 1D h - 1F h | (Reserved)    |                                |
| 20 h        | COLORCYCLE    | Color Cycle Time Period        |
| 21 h        | PELCYCLE      | Pixel Cycle Time Period        |
| 22 h        | LINECYCLE     | Line Cycle Time Period         |
| 23 h        | STEPCYCLE     | Stepper Cycle Time Period      |
| 24 h        | (Reserved)    |                                |
| 25 h        | PELSTROBE     | Pixel Strobe Control           |
| 26 h        | COLORSTART    | Color Cycle Start Offset       |
| 27 h        | PELSTART      | Pixel Cycle Start Offset       |
| 28 h        | FIRSTPEL      | First Active Pixel             |
| 29 h        | LASTPEL       | Last Active Pixel              |
| 2A h        | FIRSTLINE     | First Scan Line                |
| 2B h        | LASTLINE      | Index of Last Scan Line        |
| 2C h - 2F h | (Reserved)    |                                |

## 5.1.2 (Address 00h; MASTERCTL) Master Control

| Bits | Description   | Read | Write   | Default Value |
|------|---|------|---------|---------------|
| 15:7 | <b>Reserved.</b>  | Yes  | No      | 0             |
| 6    | <b>Session Reset.</b> Writing a 1 to this bit causes the Image Data FIFO to be flushed. The read and write FIFO pointers are reset to the value in the SRAMBASE registers. Also, the scanning logic is reset, and the SCANDONE bit ( <b>SCANSTAT[9]</b> ) is cleared. | No   | Yes/Clr | 0             |
| 5    | <b>EP81 Mode.</b> If clear, endpoint 81 returns image data from the SRAM based FIFO. If set, endpoint 81 returns SRAM data selected by the SRAMADDR register.   | Yes  | Yes     | 0             |
| 4    | <b>Pixel Diagnostic Mode.</b> If set, this bit enables a counter to provide scan data, instead of obtaining the data from the SCANDATA input pins.  | Yes  | Yes     | 0             |
| 3    | <b>Reserved.</b>  | Yes  | No      | 0             |
| 2    | <b>Enable Pixel Processing.</b> If set, this bit enables pixels to be received and processed. This bit is cleared when the <b>ABORT#</b> pin is asserted or <b>Session Reset</b> is asserted.   | Yes  | Yes     | 0             |
| 1    | <b>Enable Scanhead.</b> If set, this bit enables the scanhead signals.  | Yes  | Yes     | 0             |
| 0    | <b>Enable Stepper.</b> If set, this bit enables the stepper motor signals. This bit is cleared when the <b>ABORT#</b> pin is asserted, an end of scan is detected, <b>Session Reset</b> is asserted, or the device is suspended.                                      | Yes  | Yes     | 0             |

## 5.1.3 (Address 01h; MEMIOCTL) Memory, I/O Control

| Bits    | Description   | Read  | Write | Default Value |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
|---------|---|-------|-------|---------------|-------|-----|-------|-----|--------|-----|--------|-----|--------|---------|----------|-----|-----|---|
| 15      | <b>I/O Space Data Bus Select.</b> This bit selects which pins the data field of an I/O write request is driven out of. If clear, bits 11:0 of the USB register write value are driven out on SCANDATA[11:0]. If set, bits 7:0 of the USB register write value are driven out on SRAMDATA[7:0].  | Yes   | Yes   | 0             |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 14:12   | <b>Reserved.</b>  | Yes   | No    | 0             |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 11:8    | <b>I/O Space Access Time.</b> For I/O read cycles, this field determines the IOCS# setup time, address setup time, RD# width, address hold time, and IOCS# hold time. Note that all five of the parameters are always the same value. For I/O write cycles, this field determines the IOCS# setup time, address and data setup time, WR# width, address and data hold time, and IOCS# hold time. The access time is measured in 48-MHz clock tics, and valid values are from 1 to 15. | Yes   | Yes   | 3             |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 7       | <b>Reserved</b>   | Yes   | No    | 0             |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 6:4     | <b>SRAM Size.</b> This field determines the size of the SRAMs being used.<br><table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Value</th> <th>Size</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>32Kx8</td> </tr> <tr> <td>001</td> <td>64Kx8</td> </tr> <tr> <td>010</td> <td>128Kx8</td> </tr> <tr> <td>011</td> <td>256Kx8</td> </tr> <tr> <td>100</td> <td>512Kx8</td> </tr> <tr> <td>101-111</td> <td>reserved</td> </tr> </tbody> </table>                     | Value | Size  | 000           | 32Kx8 | 001 | 64Kx8 | 010 | 128Kx8 | 011 | 256Kx8 | 100 | 512Kx8 | 101-111 | reserved | Yes | Yes | 0 |
| Value   | Size  |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 000     | 32Kx8   |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 001     | 64Kx8   |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 010     | 128Kx8  |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 011     | 256Kx8  |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 100     | 512Kx8  |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 101-111 | reserved  |       |       |               |       |     |       |     |        |     |        |     |        |         |          |     |     |   |
| 3:0     | <b>SRAM Access Time.</b> For SRAM read cycles, this field determines the width of the SRAMCS[3:0]# and RD# controls. For SRAM write cycles, this field determines the width of the SRAMCS[3:0]# and WR# controls. The access time is measured in 48-MHz clock tics, and valid values are from 1 to 15.  | Yes   | Yes   | 2             |       |     |       |     |        |     |        |     |        |         |          |     |     |   |

## 5.1.4 (Address 02h; PIXCTL) Pixel Control

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:5 | <b>Reserved.</b>   | Yes  | No    | 0             |
| 4    | <b>BW/Color.</b> If clear, the color mode is selected. If set, the black and white or grayscale mode is selected.  | Yes  | Yes   | 0             |
| 3:0  | <b>Bit Depth.</b> This field selects the number of bits returned to the host for each color (color mode) or pixel (black and white or grayscale mode). The least significant bits from the SCANDATA bus are selected. If the BW/Color bit is cleared (color mode), valid values for this field are 8, 10, and 12. If the BW/Color bit is set (black and white or grayscale mode), valid values for this field are 8, 10, and 12. | Yes  | Yes   | 0x8           |

## 5.1.5 (Address 03h; IOCFG) I/O Pin Configuration

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15   | <b>GIOPEL3 Direction.</b> If clear, this pin is an input. If set, this pin is an output.   | Yes  | Yes   | 0             |
| 14   | <b>GIOPEL2 Direction.</b> If clear, this pin is an input. If set, this pin is an output.   | Yes  | Yes   | 0             |
| 13   | <b>GIOPEL1 Direction.</b> If clear, this pin is an input. If set, this pin is an output.   | Yes  | Yes   | 0             |
| 12   | <b>GIOPEL0 Direction.</b> If clear, this pin is an input. If set, this pin is an output.   | Yes  | Yes   | 0             |
| 11   | <b>GIOLINE3 Direction.</b> If clear, this pin is an input. If set, this pin is an output.  | Yes  | Yes   | 0             |
| 10   | <b>GIOLINE2 Direction.</b> If clear, this pin is an input. If set, this pin is an output.  | Yes  | Yes   | 0             |
| 9    | <b>GIOLINE1 Direction.</b> If clear, this pin is an input. If set, this pin is an output.  | Yes  | Yes   | 0             |
| 8    | <b>GIOLINE0 Direction.</b> If clear, this pin is an input. If set, this pin is an output.  | Yes  | Yes   | 0             |
| 7    | <b>GIOPEL3 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs.  | Yes  | Yes   | 0             |
| 6    | <b>GIOPEL2 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs.  | Yes  | Yes   | 0             |
| 5    | <b>GIOPEL1 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs.  | Yes  | Yes   | 0             |
| 4    | <b>GIOPEL0 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs.  | Yes  | Yes   | 0             |
| 3    | <b>GIOLINE3 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs. | Yes  | Yes   | 0             |
| 2    | <b>GIOLINE2 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs. | Yes  | Yes   | 0             |
| 1    | <b>GIOLINE1 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs. | Yes  | Yes   | 0             |
| 0    | <b>GIOLINE0 Output Type.</b> If clear, this pin is a digital output. If set, this pin is a PWM output. This field only affects I/O pins configured as outputs. | Yes  | Yes   | 0             |

## 5.1.6 (Address 04h; SCANSTAT) Scanner Status

| Bits  | Description   | Read | Write   | Default Value |
|-------|---|------|---------|---------------|
| 15:10 | <b>Reserved.</b>  | Yes  | No      | 0             |
| 9     | <b>Scan Done.</b> If set, this bit indicates that a scan has completed. Once this bit is set, no scan data is written to SRAM, and the stepper enable bit ( <b>MASTERCTL[0]</b> ) is cleared. The line counter will not increment while this bit is set. The assertion of <b>Session Reset</b> clears this bit. | Yes  | No      | 0             |
| 8     | <b>Transmit FIFO Overflow.</b> If set, this bit indicates that an attempt was made by the scanner logic to write to the SRAM transmit FIFO when the transmit FIFO was full. The assertion of <b>Session Reset</b> clears this bit.  | Yes  | No      | 0             |
| 7     | <b>Scan Abort.</b> The most recent scan was aborted due to the assertion of the ABORT# pin. Writing a 1 clears this bit if the ABORT# pin is not active.  | Yes  | Yes/Clr | 0             |
| 6     | <b>Data Pending.</b> There is image data in the SRAM FIFO waiting to be sent. The assertion of <b>Session Reset</b> clears this bit.  | Yes  | No      | 0             |
| 5     | <b>Transmit FIFO Full.</b> If set, this bit indicates that the SRAM transmit FIFO is full. The assertion of <b>Session Reset</b> clears this bit.   | Yes  | No      | 0             |
| 4     | <b>Reserved.</b>  | Yes  | No      | 0             |
| 3     | <b>Scan Half-Speed.</b> An in-progress scan is currently progressing at ½ speed because the FIFO count crossed the FIFO half-speed scan threshold. The scan will resume at full speed when the FIFO count is lower than the full-speed scan threshold.  | Yes  | No      | 0             |
| 2     | <b>Scan Pixel FIFO Overflow.</b> If set, this bit indicates that the 4-byte pixel FIFO has overflowed. The assertion of <b>Session Reset</b> clears this bit.   | Yes  | No      | 0             |
| 1     | <b>Scan Flow Control Stop.</b> An in-progress scan will be stopped at the end of the current line because the FIFO count crossed the FIFO stop threshold. The scan resumes when the FIFOFSTHR threshold is reached.   | Yes  | No      | 0             |
| 0     | <b>Reset.</b> The NET1031 is currently being reset. This bit will never read as a '1' since register reads are not possible during Reset time; however, the corresponding change bit in SCANCHG will remain active until cleared to indicate that the NET1031 has been reset.                                   | Yes  | No      | 0             |

## 5.1.7 (Address 05h; IOSTAT) I/O Pin Status

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:8 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 7    | <b>GIOPEL3.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output.  | Yes  | Yes   | 1             |
| 6    | <b>GIOPEL2.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output.  | Yes  | Yes   | 1             |
| 5    | <b>GIOPEL1.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output.  | Yes  | Yes   | 1             |
| 4    | <b>GIOPEL0.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output.  | Yes  | Yes   | 1             |
| 3    | <b>GIOLINE3.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output. | Yes  | Yes   | 1             |
| 2    | <b>GIOLINE2.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output. | Yes  | Yes   | 1             |
| 1    | <b>GIOLINE1.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output. | Yes  | Yes   | 1             |
| 0    | <b>GIOLINE0.</b> The value of this bit reflects the current state of this I/O pin. A register write to this bit will be driven out of this pin if it is configured as a digital output. | Yes  | Yes   | 1             |

### 5.1.8 (Address 06h; SCANCHG) Scanner Status Change Register

Each bit in this register reports a change in the corresponding bit of SCANSTAT. Each bit in this register may be cleared by writing a '1' to the corresponding bit. All bits are cleared when **Session Reset** is asserted. This register contains the same information as the first word sent by the Status endpoint. The default value is 0x0021.

### 5.1.9 (Address 07h; IOCHG) I/O Pin Status Change Register

Each bit in this register reports a change in the corresponding bit of IOSTAT. Each bit in this register may be cleared by writing a '1' to the corresponding bit. All bits are cleared when **Session Reset** is asserted. This register contains the same information as the second word sent by the Status endpoint. The default value is 0x00FF.

### 5.1.10 (Address 08h; SRAMADDR1) SRAM Address, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>SRAM Address MSW.</b> These bits specify the most significant bits of the initial SRAM address when accessed through endpoints 1 (SRAM write) or 81 (SRAM read). | Yes  | Yes   | 0             |

### 5.1.11 (Address 09h; SRAMADDR0) SRAM Address, Least-Significant Word

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>SRAM Address LSW.</b> These bits specify the least significant bits of the initial SRAM address when accessed through endpoints 1 (SRAM write) or 81 (SRAM read). The 21-bit SRAM address is incremented after each access. | Yes  | Yes   | 0             |

### 5.1.12 (Address 0Ah - 0Fh; RESERVED) Reserved for future use

### 5.1.13 (Address 10h; SRAMBASE1) SRAM FIFO Address Base, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>SRAM FIFO Address Base MSW.</b> These bits specify the most significant bits of the first address above the PRNU correction table in the external SRAM connected to the NET1031. This address corresponds to the beginning of the SRAM FIFO. | Yes  | Yes   | 0             |

### 5.1.14 (Address 11h; SRAMBASE0) SRAM FIFO Address Base, Least-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>SRAM FIFO Address Base LSW.</b> These bits specify the most significant bits of the first address above the PRNU correction table in the external SRAM connected to the NET1031. This address corresponds to the beginning of the SRAM FIFO. | Yes  | Yes   | 1             |

### 5.1.15 (Address 12h; SRAMTOP1) SRAM FIFO Address Top, Most-Significant Word

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:5 | <b>Reserved.</b>   | Yes  | No    | 0             |
| 4:0  | <b>SRAM FIFO Address Top MSW.</b> These bits specify the most significant bits of the last address in the external SRAM used for the image FIFO. This address corresponds to the end of the SRAM image FIFO. | Yes  | Yes   | 0             |

### 5.1.16 (Address 13h; SRAMTOP0) SRAM FIFO Address Top, Least-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>SRAM FIFO Address Top LSW.</b> These bits specify the least significant bits of the last address in the external SRAM used for the image FIFO. This address corresponds to the end of the SRAM image FIFO. | Yes  | Yes   | 0x7fff        |

### 5.1.17 (Address 14h; FIFOFSTHR1) FIFO Full-Speed Threshold, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>FIFO Full-Speed Threshold, MSW.</b> This value is the SRAM FIFO count below which a scan will resume at full speed. The speed change occurs only at the end of a line. | Yes  | Yes   | 0             |

### 5.1.18 (Address 15h; FIFOFSTHR0) FIFO Full-Speed Threshold, Least-Significant Word

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>FIFO Full-Speed Threshold, LSW.</b> This value is the SRAM FIFO count below which a scan will resume at full speed. The speed change occurs only at the end of a line. By setting this threshold lower than the half-speed threshold, a hysteresis effect is introduced which helps to prevent a scanner from slowing down and speeding up frequently during an image scan. | Yes  | Yes   | 0x0060        |

### 5.1.19 (Address 16h; FIFOHSTHR1) FIFO Half-Speed Threshold, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>FIFO Half-Speed Threshold, MSW.</b> This value is the SRAM FIFO count above which the scan will slow to half -speed to reduce the data acquisition rate. The speed change occurs only at the end of a line. The scan will resume at full speed when the FIFO count has gone below the "FIFO Full-Speed Threshold". | Yes  | Yes   | 0x1F          |



### 5.1.20 (Address 17h; FIFOHSTHR0) FIFO Half-Speed Threshold, Least-Significant Word

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>FIFO Half-Speed Threshold, LSW.</b> This value is the SRAM FIFO count above which the scan will slow to half-speed to reduce the data acquisition rate. The speed change occurs only at the end of a line. The scan will resume at full speed when the FIFO count has gone below the "FIFO Full-Speed Threshold". | Yes  | Yes   | 0xFFFF        |

### 5.1.21 (Address 18h; FIFOSTOPTHR1) FIFO Stop Threshold, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>FIFO Stop Threshold, MSW.</b> This value is the SRAM FIFO count above which the scanner will stop scanning. This prevents an image buffer overflow. The scanner stops at the end of a line, so this threshold should be set one line's worth of data below the top of memory. The scan will resume at full speed when the FIFO count has gone below the "FIFO Full-Speed Threshold". | Yes  | Yes   | 0             |

### 5.1.22 (Address 19h; FIFOSTOPTHR0) FIFO Stop Threshold, Least-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>FIFO Stop Threshold, LSW.</b> This value is the SRAM FIFO count above which the scanner will stop scanning. This prevents an image buffer overflow. The scanner stops at the end of a line, so this threshold should be set one line's worth of data below the top of memory. The scan will resume at full speed when the FIFO count has gone below the "FIFO Full-Speed Threshold". | Yes  | Yes   | 0x4000        |

### 5.1.23 (Address 1Ah; FIFOCOUNT1) FIFO Byte Count, Most-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4:0  | <b>FIFO Byte Count, MSW.</b> This value is the number of bytes in the FIFO. | Yes  | No    | 0x0           |

### 5.1.24 (Address 1Bh; FIFOCOUNT0) FIFO Byte Count, Least-Significant Word

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>FIFO Byte Count, LSW.</b> This value is the number of bytes in the FIFO. | Yes  | No    | 0x0           |

## 5.1.25 (Address 1Ch; FIFOSTAT) FIFO Status

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:5 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 4    | <b>Transmit FIFO Full-Speed Threshold.</b> If set, this bit indicates that the SRAM transmit FIFO count is less than the Full-Speed Threshold.    | Yes  | No    | 0             |
| 3    | <b>Transmit FIFO Half-Speed Threshold.</b> If set, this bit indicates that the SRAM transmit FIFO count is greater than the Half-Speed Threshold. | Yes  | No    | 0             |
| 2    | <b>Transmit FIFO Stop Threshold.</b> If set, this bit indicates that the SRAM transmit FIFO count is greater than the Stop Threshold.             | Yes  | No    | 0             |
| 1    | <b>Transmit FIFO Full.</b> If set, this bit indicates that the SRAM transmit FIFO is full.  | Yes  | No    | 0             |
| 0    | <b>Transmit FIFO Empty.</b> If set, this bit indicates that the SRAM transmit FIFO is empty.  | Yes  | No    | 1             |

## 5.1.26 (Address 1Dh - 1Fh; RESERVED) Reserved for future use

## 5.1.27 (Address 20h; COLORCYCLE) Color Cycle Time Period

| Bits  | Description   | Read | Write | Default Value |
|-------|---|------|-------|---------------|
| 15:10 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 9:0   | <b>Color Cycle Period.</b> The value in this register is the number of 48-MHz clock tics allocated to each color. | Yes  | Yes   | 0x020         |

## 5.1.28 (Address 21h; PELCYCLE) Pixel Cycle Time Period

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:3 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 2:0  | <b>Pixel Cycle Period.</b> The value in this register is the number of color cycles allocated to each pixel. This value is normally '1' for monochrome and '3' for RGB. | Yes  | Yes   | 0x3           |

## 5.1.29 (Address 22h; LINECYCLE) Line Cycle Time Period

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15   | <b>Reserved.</b>  | Yes  | No    | 0             |
| 14:0 | <b>Line Cycle Period.</b> The value in this register is the number of pixel cycles allocated to line-based signals. | Yes  | Yes   | 0x2000        |

## 5.1.30 (Address 23h; STEPCYCLE) Stepper Cycle Time Period

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15   | <b>Reserved.</b>  | Yes  | No    | 0             |
| 14:0 | <b>Stepper Cycle Period.</b> The value in this register is the number of pixel cycles allocated to stepper motor signals. | Yes  | Yes   | 0x1c98        |

## 5.1.31 (Address 25h; PELSTROBE) Pixel Strobe

| Bits  | Description   | Read | Write | Default Value |
|-------|---|------|-------|---------------|
| 15:10 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 9:0   | <p><b>Pixel Strobe Offset.</b> The value of these bits is the offset at which the image data at the SCANDATA input pins is valid. The offset is counted in 48 MHz clock cycles from the beginning of a color or pixel cycle, depending on the <b>PIXCTL[4]</b> bit. For black and white mode, a pixel strobe occurs once per pixel, and the offset is based from the beginning of the pixel cycle. For color mode, a pixel strobe occurs once per color cycle, and the pixel strobe offset is based from the beginning of the color cycle. The valid range is from 1 to 1023.</p> <p>The PELSTROBE output pin can be used for diagnostics to determine when pixel data is being captured.</p> | Yes  | Yes   | 0x004         |

## 5.1.32 (Address 26h; COLORSTART) Color Cycle Start Offset

| Bits  | Description   | Read | Write | Default Value |
|-------|---|------|-------|---------------|
| 15:10 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 9:0   | <p><b>Color Cycle Start Offset.</b> The value in this register specifies the number of 48-MHz clock cycles at the beginning of a pixel before color-based waveforms should begin cycling. The valid range is from 1 to 1023. If 0, no offset is inserted.</p> | Yes  | Yes   | 0             |

## 5.1.33 (Address 27h; PELSTART) Pixel Cycle Start Offset

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15   | <b>Reserved.</b>  | Yes  | No    | 0             |
| 14:0 | <p><b>Pixel Cycle Start Offset.</b> The value in this register specifies the number of pixel cycles at the beginning of a line before pixel-based waveforms should begin cycling. The valid range is from 1 to 1023. If 0, no offset is inserted.</p> | Yes  | Yes   | 0x000e        |

## 5.1.34 (Address 28h; FIRSTPEL) First Active Pixel

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15   | <b>Reserved.</b>  | Yes  | No    | 0             |
| 14:0 | <p><b>First Active Pixel.</b> The first pixel in the CCD / CIS sensor's active window. Pixels before this index are clocked out of the CCD / CIS, but not stored by the NET1031. This is used to perform horizontal cropping in hardware.</p> | Yes  | Yes   | 0x0041        |

## 5.1.35 (Address 29h; LASTPEL) Last Active Pixel

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15   | <b>Reserved.</b>   | Yes  | No    | 0             |
| 14:0 | <p><b>Last Active Pixel.</b> The last pixel in the CCD / CIS sensor's active window. Pixels after this index and before a line cycle are clocked out of the CCD / CIS, but not stored by the NET1031. This is used to perform horizontal cropping in hardware.</p> | Yes  | Yes   | 0x14f5        |

## 5.1.36 (Address 2Ah; FIRSTLINE) First Scan Line

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15   | <b>Reserved.</b>  | Yes  | No    | 0             |
| 14:0 | <b>First Scan Line to Store.</b> The first line number that should be stored by the NET1031. For line numbers before this value, the scanhead signals are active, but scanned data is not stored by the NET1031. This is used to perform vertical cropping in hardware. | Yes  | Yes   | 0x0001        |

## 5.1.37 (Address 2Bh; LASTLINE) Last Scan Line

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15   | <b>Reserved.</b>   | Yes  | No    | 0             |
| 14:0 | <b>Last Line to Store.</b> The line at which scanning should stop. Lines after this value are not stored by the NET1031. This is used to perform vertical cropping in hardware. Upon reaching this threshold, the enable stepper bit in the master control register ( <b>MASTERCTL[0]</b> ) is cleared, the scan done bit ( <b>SCANSTAT[9]</b> ) is set, and data is no longer stored into the FIFO. Note: n-1 lines are actually transferred. | Yes  | Yes   | 0x0800        |

## 5.2 Pixel-based Waveform Register Description

The PWM signal registers configure the various PWM output pins of the NET1031. A set of registers is associated with each PWM output pin. Note that the names associated with each signal are arbitrary. Any PWM pin associated with these registers can be used for any scanner function requiring a pixel-based or digital output signal. Refer to section 9.1.1 for a timing diagram of a pixel-based output.

### 5.2.1 Pixel-based Waveform Register Summary

| Address     | Register Name | Register Description   | Default Value |
|-------------|---------------|--|---------------|
| 40 h        | ADCCLKHIGH    | Analog-to-Digital Converter clock, high delay                    | 0x0001        |
| 41 h        | ADCCLKLOW     | Analog-to-Digital Converter clock, low delay                     | 0x0006        |
| 42 h        | ADCCLKCTL     | Analog-to-Digital Converter clock, waveform control              | 0x0002        |
| 43 h        | REFNHIGH      | Analog-to-Digital Converter negative reference, high delay       | 0x0000        |
| 44 h        | REFNLOW       | Analog-to-Digital Converter negative reference, low delay        | 0x0000        |
| 45 h        | REFNCTL       | Analog-to-Digital Converter negative reference, waveform control | 0x0008        |
| 46 h        | REFPHIGH      | Analog-to-Digital Converter positive reference, high delay       | 0x0000        |
| 47 h        | REFPLOW       | Analog-to-Digital Converter positive reference, low delay        | 0x0000        |
| 48 h        | REFPCTL       | Analog-to-Digital Converter positive reference, waveform control | 0x0008        |
| 49 h        | GAINHIGH      | Analog-to-Digital Converter gain control, high delay             | 0x0000        |
| 4A h        | GAINLOW       | Analog-to-Digital Converter gain control, low delay              | 0x0000        |
| 4B h        | GAINCTL       | Analog-to-Digital Converter gain control, waveform control       | 0x0008        |
| 4C h        | OFFSETHIGH    | Analog-to-Digital Converter offset control, high delay           | 0x0000        |
| 4D h        | OFFSETLOW     | Analog-to-Digital Converter offset control, low delay            | 0x0000        |
| 4E h        | OFFSETCTL     | Analog-to-Digital Converter offset control, waveform control     | 0x0008        |
| 4F h        | CLAMPHIGH     | Analog-to-Digital Converter clamp control, high delay            | 0x0000        |
| 50 h        | CLAMPLOW      | Analog-to-Digital Converter clamp control, low delay             | 0x0000        |
| 51 h        | CLAMPCTL      | Analog-to-Digital Converter clamp control, waveform control      | 0x0008        |
| 52 h        | SH1HIGH       | Analog-to-Digital Converter sample/hold 1, high delay            | 0x0006        |
| 53 h        | SH1LOW        | Analog-to-Digital Converter sample/hold 1, low delay             | 0x000f        |
| 54 h        | SH1CTL        | Analog-to-Digital Converter sample/hold 1, waveform control      | 0x0008        |
| 55 h        | SH2HIGH       | Analog-to-Digital Converter sample/hold 2, high delay            | 0x0026        |
| 56 h        | SH2LOW        | Analog-to-Digital Converter sample/hold 2, low delay             | 0x0045        |
| 57 h        | SH2CTL        | Analog-to-Digital Converter sample/hold 2, waveform control      | 0x0008        |
| 58 h        | PHI1HIGH      | CCD Clock 1, high delay  | 0x0013        |
| 59 h        | PHI1LOW       | CCD Clock 1, low delay   | 0x0002        |
| 5A h        | PHI1CTL       | CCD Clock 1, waveform control                                    | 0x0008        |
| 5B h        | PHI2HIGH      | CCD Clock 2, high delay  | 0x0003        |
| 5C h        | PHI2LOW       | CCD Clock 2, low delay   | 0x0014        |
| 5D h        | PHI2CTL       | CCD Clock 2, waveform control                                    | 0x0009        |
| 5E h        | RS1HIGH       | CCD Reset 1 / CIS Clock, high delay                              | 0x0002        |
| 5F h        | RS1LOW        | CCD Reset 1 / CIS Clock, low delay                               | 0x0007        |
| 60 h        | RS1CTL        | CCD Reset 1 / CIS Clock, waveform control                        | 0x0001        |
| 61 h        | RS2HIGH       | CCD Reset 2, high delay  | 0x0008        |
| 62 h        | RS2LOW        | CCD Reset 2, low delay   | 0x000d        |
| 63 h        | RS2CTL        | CCD Reset 2, waveform control                                    | 0x0001        |
| 64 h        | MUX0HIGH      | Analog-to-Digital Converter mux control bit 0, high delay        | 0x0000        |
| 65 h        | MUX0LOW       | Analog-to-Digital Converter mux control bit 0, low delay         | 0x0000        |
| 66 h        | MUX0CTL       | Analog-to-Digital Converter mux control bit 0, waveform control  | 0x0001        |
| 67 h        | MUX1HIGH      | Analog-to-Digital Converter mux control bit 1, high delay        | 0x0000        |
| 68 h        | MUX1LOW       | Analog-to-Digital Converter mux control bit 1, low delay         | 0x0000        |
| 69 h        | MUX1CTL       | Analog-to-Digital Converter mux control bit 1, waveform control  | 0x0008        |
| 6A h - 7F h | (Reserved)    |  |               |
| 80 h        | GIOPELOHIGH   | Pixel based general I/O bit 0, high delay                        | 0x0000        |

| Address     | Register Name | Register Description                            | Default Value |
|-------------|---------------|---|---------------|
| 81 h        | GIOPEL0LOW    | Pixel based general I/O bit 0, low delay        | 0x0000        |
| 82 h        | GIOPEL0CTL    | Pixel based general I/O bit 0, waveform control | 0x0008        |
| 83 h        | GIOPEL1HIGH   | Pixel based general I/O bit 1, high delay       | 0x0000        |
| 84 h        | GIOPEL1LOW    | Pixel based general I/O bit 1, low delay        | 0x0000        |
| 85 h        | GIOPEL1CTL    | Pixel based general I/O bit 1, waveform control | 0x0008        |
| 86 h        | GIOPEL2HIGH   | Pixel based general I/O bit 2, high delay       | 0x0000        |
| 87 h        | GIOPEL2LOW    | Pixel based general I/O bit 2, low delay        | 0x0000        |
| 88 h        | GIOPEL2CTL    | Pixel based general I/O bit 2, waveform control | 0x0008        |
| 89 h        | GIOPEL3HIGH   | Pixel based general I/O bit 3, high delay       | 0x0000        |
| 8A h        | GIOPEL3LOW    | Pixel based general I/O bit 3, low delay        | 0x0000        |
| 8B h        | GIOPEL3CTL    | Pixel based general I/O bit 3, waveform control | 0x0008        |
| 8C h - 8F h | (Reserved)    |   |               |

### 5.2.2 (xxxxHIGH) Pixel-based Waveform High Offset

| Bits  | Description  | Read | Write |
|-------|--|------|-------|
| 15:10 | <b>Reserved.</b>   | Yes  | No    |
| 9:0   | <b>Waveform High Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to high. The value is defined in units of 48-MHz clock ticks for color- and pixel-based signals. If <b>Waveform High Offset</b> is set equal to <b>Waveform Low Offset</b> , then the pin is treated as a digital output. The Initial Polarity field in the xxxxCTL register determines the value of the digital output. | Yes  | Yes   |

### 5.2.3 (xxxxLOW) Pixel-based Waveform Low Offset

| Bits  | Description  | Read | Write |
|-------|--|------|-------|
| 15:10 | <b>Reserved.</b>   | Yes  | No    |
| 9:0   | <b>Waveform Low Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to low. | Yes  | Yes   |

### 5.2.4 (xxxxCTL) Pixel-based Waveform Control

| Bits | Description   | Read | Write |
|------|---|------|-------|
| 15:4 | <b>Reserved.</b>  | Yes  | No    |
| 3    | <b>Pause Enable.</b> If clear, this PWM output does not pause during a scan. If set, this PWM output pauses based on PELSTART and COLORSTART.   | Yes  | Yes   |
| 2    | <b>Open-Drain/Totem-Pole Output.</b> If this waveform is configured as an output, clearing this bit configures the waveform to be a totem-pole output. If the bit is set, the waveform is open-drain (i.e. not driven when the waveform is high). | Yes  | Yes   |
| 1    | <b>Color Cycle Select.</b> If clear, this signal cycles on a pixel cycle. If set, this waveform cycles on a color cycle.  | Yes  | Yes   |
| 0    | <b>Initial Polarity.</b> This bit determines the state of the PWM signal (high or low) while it is not enabled ( <b>MASTERCTL[1] = 0</b> ) or while it is configured as a digital output.   | Yes  | Yes   |

### 5.3 Line-based Waveform Register Description

The PWM signal registers configure the various PWM output pins of the NET1031. A set of registers is associated with each PWM output pin. Any PWM pin associated with these registers can be used for any scanner function requiring a line-based signal or a digital output. Refer to section 9.1.1 for a timing diagram of a line-based output.

#### 5.3.1 Line-based Waveform Register Summary

| Address     | Register Name | Register Description  | Default Value |
|-------------|---------------|---|---------------|
| 90 h        | LEDRHIGH      | Red lamp waveform for sequential color scan, high delay         | 0x0000        |
| 91 h        | LEDRLOW       | Red lamp waveform for sequential color scan, low delay          | 0x0000        |
| 92 h        | LEDRCTL       | Red lamp waveform for sequential color scan, waveform control   | 0x0000        |
| 93 h        | LEDGHIGH      | Green lamp waveform for sequential color scan, high delay       | 0x0000        |
| 94 h        | LEDGLOW       | Green lamp waveform for sequential color scan, low delay        | 0x0000        |
| 95 h        | LEDGCTL       | Green lamp waveform for sequential color scan, waveform control | 0x0000        |
| 96 h        | LEDBHIGH      | Blue lamp waveform for sequential color scan, high delay        | 0x0000        |
| 97 h        | LEDBLOW       | Blue lamp waveform for sequential color scan, low delay         | 0x0000        |
| 98 h        | LEDBCTL       | Blue lamp waveform for sequential color scan, waveform control  | 0x0000        |
| 99 h        | SG1HIGH       | CCD Shift Gate 1, high delay                                    | 0x001b        |
| 9A h        | SG1LOW        | CCD Shift Gate 1, low delay                                     | 0x0010        |
| 9B h        | SG1CTL        | CCD Shift Gate 1, waveform control                              | 0x0001        |
| 9C h        | SG2HIGH       | CCD Shift Gate 2, high delay                                    | 0x000e        |
| 9D h        | SG2LOW        | CCD Shift Gate 2, low delay                                     | 0x0001        |
| 9E h        | SG2CTL        | CCD Shift Gate 2, waveform control                              | 0x0001        |
| 9F h - BF h | (Reserved)    |   |               |
| C0 h        | GIOLINE0HIGH  | Line based general I/O bit 0, high delay                        | 0x0000        |
| C1 h        | GIOLINE0LOW   | Line based general I/O bit 0, low delay                         | 0x0000        |
| C2 h        | GIOLINE0CTL   | Line based general I/O bit 0, waveform control                  | 0x0000        |
| C3 h        | GIOLINE1HIGH  | Line based general I/O bit 1, high delay                        | 0x0000        |
| C4 h        | GIOLINE1LOW   | Line based general I/O bit 1, low delay                         | 0x0000        |
| C5 h        | GIOLINE1CTL   | Line based general I/O bit 1, waveform control                  | 0x0000        |
| C6 h        | GIOLINE2HIGH  | Line based general I/O bit 2, high delay                        | 0x0000        |
| C7 h        | GIOLINE2LOW   | Line based general I/O bit 2, low delay                         | 0x0000        |
| C8 h        | GIOLINE2CTL   | Line based general I/O bit 2, waveform control                  | 0x0000        |
| C9 h        | GIOLINE3HIGH  | Line based general I/O bit 3, high delay                        | 0x0000        |
| CA h        | GIOLINE3LOW   | Line based general I/O bit 3, low delay                         | 0x0000        |
| CB h        | GIOLINE3CTL   | Line based general I/O bit 3, waveform control                  | 0x0000        |
| CC h - CF h | (Reserved)    |   |               |

## 5.3.2 (xxxxHIGH) Line-based Waveform High Offset

| Bits | Description  | Read | Write |
|------|--|------|-------|
| 15   | <b>Reserved.</b>   | Yes  | No    |
| 14:0 | <b>Waveform High Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to high. The value is defined in units of pixels for line- and step-based signals. If <b>Waveform High Offset</b> is set equal to <b>Waveform Low Offset</b> , then the pin is treated as a digital output. The Initial Polarity field in the xxxxCTL register determines the value of the digital output. | Yes  | Yes   |

## 5.3.3 (xxxxLOW) Line-based Waveform Low Offset

| Bits | Description  | Read | Write |
|------|--|------|-------|
| 15   | <b>Reserved.</b>   | Yes  | No    |
| 14:0 | <b>Waveform Low Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to low. The value is defined in units of pixels for line- and step-based signals. | Yes  | Yes   |

## 5.3.4 (xxxxCTL) Line-based Waveform Control

| Bits | Description   | Read | Write |
|------|---|------|-------|
| 15:3 | <b>Reserved.</b>  | Yes  | No    |
| 2    | <b>Open-Drain/Totem-Pole Output.</b> If this waveform is configured as an output, clearing this bit configures the waveform to be a totem-pole output. If the bit is set, the waveform is open-drain (i.e. not driven when the waveform is high). | Yes  | Yes   |
| 1    | <b>Reserved.</b>  | Yes  | No    |
| 0    | <b>Initial Polarity.</b> This bit determines the state of the PWM signal (high or low) while it is not enabled ( <b>MASTERCTL[1] = 0</b> ) or while it is configured as a digital output.   | Yes  | Yes   |



## 5.4 Stepper-based Waveform Register Description

The PWM signal registers configure the various PWM output pins of the NET1031. A set of registers is associated with each PWM output pin. Any PWM pin associated with these registers can be used for any scanner function requiring a stepper-based signal or a digital output. The STEPCYCLE register controls the number of pixel cycles over which stepper-based signals cycle. Refer to section 9.1.1 for a timing diagram of a line/stepper-based output.

### 5.4.1 Stepper-based Waveform Register Summary

| Address     | Register Name | Register Description   | Default Value |
|-------------|---------------|--|---------------|
| D0 h        | MVRHIGH       | Stepper Motor throttle, high delay                               | 0x0000        |
| D1 h        | MVRLOW        | Stepper Motor throttle, low delay                                | 0x0000        |
| D2 h        | MVRCTL        | Stepper Motor throttle, waveform control                         | 0x0000        |
| D3 h        | PIHIGH        | Stepper Motor energize phase 1, high delay                       | 0x0001        |
| D4 h        | PILOW         | Stepper Motor energize phase 1, low delay                        | 0x3000        |
| D5 h        | P1CTL         | Stepper Motor energize phase 1, waveform control                 | 0x0000        |
| D6 h        | P2HIGH        | Stepper Motor energize phase 2, high delay                       | 0x6000        |
| D7 h        | P2LOW         | Stepper Motor energize phase 2, low delay                        | 0x1000        |
| D8 h        | P2CTL         | Stepper Motor disable phase 2, waveform control                  | 0x0000        |
| D9 h        | DS1HIGH       | Stepper Motor disable phase 1, high delay                        | 0x2000        |
| DA h        | DS1LOW        | Stepper Motor disable phase 1, low delay                         | 0x5000        |
| DB h        | DS1CTL        | Stepper Motor disable phase 1, waveform control                  | 0x0000        |
| DC h        | DS2HIGH       | Stepper Motor disable phase 2, high delay                        | 0x4000        |
| DD h        | DS2LOW        | Stepper Motor disable phase 2, low delay                         | 0x7000        |
| DE h        | DS2CTL        | Stepper Motor disable phase 2, waveform control                  | 0x0000        |
| DF h        | S0HIGH        | Stepper Motor voltage reference selector bit 0, high delay       | 0x0000        |
| E0 h        | S0LOW         | Stepper Motor voltage reference selector bit 0, low delay        | 0x0000        |
| E1 h        | S0CTL         | Stepper Motor voltage reference selector bit 0, waveform control | 0x0000        |
| E2 h        | S1HIGH        | Stepper Motor voltage reference selector bit 1, high delay       | 0x0000        |
| E3 h        | S1LOW         | Stepper Motor voltage reference selector bit 1, low delay        | 0x0000        |
| E4 h        | S1CTL         | Stepper Motor voltage reference selector bit 1, waveform control | 0x0000        |
| E5 h - EF h | (Reserved)    |  |               |

## 5.4.2 (xxxxHIGH) Stepper-based Waveform High Offset

| Bits | Description   | Read | Write |
|------|---|------|-------|
| 15   | <b>Reserved.</b>  | Yes  | No    |
| 14:0 | <b>Waveform High Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to high. The value is defined in units of pixels for stepper-based signals. If <b>Waveform High Offset</b> is set equal to <b>Waveform Low Offset</b> , then the pin is treated as a digital output. The Initial Polarity field in the xxxxCTL register determines the value of the digital output. | Yes  | Yes   |

## 5.4.3 (xxxxLOW) Stepper-based Waveform Low Offset

| Bits | Description   | Read | Write |
|------|---|------|-------|
| 15   | <b>Reserved.</b>  | Yes  | No    |
| 14:0 | <b>Waveform Low Offset.</b> Defines the offset after the cycle start that a PWM signal transitions to low. The value is defined in units of pixels for stepper-based signals. | Yes  | Yes   |

## 5.4.4 (xxxxCTL) Stepper-based Waveform Control

| Bits | Description   | Read | Write |
|------|---|------|-------|
| 15:3 | <b>Reserved.</b>  | Yes  | No    |
| 2    | <b>Open-Drain/Totem-Pole Output.</b> If this waveform is configured as an output, clearing this bit configures the waveform to be a totem-pole output. If the bit is set, the waveform is open-drain (i.e. not driven when the waveform is high). | Yes  | Yes   |
| 1    | <b>Reserved.</b>  | Yes  | No    |
| 0    | <b>Initial Polarity.</b> This bit determines the state of the PWM signal (high or low) while it is not enabled ( <b>MASTERCCTL[1] = 0</b> ) or while it is configured as a digital output.  | Yes  | Yes   |

## 5.5 USB Register Description

These registers determine some of the values reported in USB device and configuration descriptors returned to the host. The values in the registers may be changed by the initialization interface before a descriptor is returned to the host. See Section 3.5.

### 5.5.1 USB Register Summary

| Address Range | Register Set   | Register Set Description                       |
|---------------|----------------|--|
| F0 h          | Vendor ID      | USB Vendor ID Field                            |
| F1 h          | Product ID     | USB Product ID Field                           |
| F2 h          | Release Number | USB Device release number                      |
| F3 h          | Max Power      | Maximum USB power used                         |
| F4 h          | USBCTL1        | USB control 1                                  |
| F5 h          | USBCTL2        | USB control 2                                  |
| F6 h          | STRINDEX1      | USB String Index 1 (Language ID, Manufacturer) |
| F7 h          | STRINDEX2      | USB String Index 2 (Product, Serial Number)    |
| F8-FB h       | Reserved       |  |
| FC h          | EECTL          | EEPROM Control                                 |
| FD h          | EEADDR         | EEPROM Address                                 |
| FE h          | EEDATA         | EEPROM Data                                    |
| FF h          | Revision       | Current Silicon Revision                       |

### 5.5.2 (Address F0h; VID) Vendor ID

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>Vendor ID.</b> This register determines the Vendor ID during a 'Get Device Descriptor' request. | Yes  | Yes   | 0x0525        |

### 5.5.3 (Address F1h; PID) Product ID

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>Product ID.</b> This register determines the Product ID during a 'Get Device Descriptor' request. | Yes  | Yes   | 0x1031        |

### 5.5.4 (Address F2h; REL) Release Number

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>Release Number.</b> This register determines the device release number during a 'Get Device Descriptor' request. | Yes  | Yes   | REL NUM       |

Note: RELNUM is the silicon revision, encoded as a 4-digit BCD value. The value of RELNUM for the first release of the chip is 0x0100. The least-significant two digits are incremented for mask changes, and the most-significant two digits increment for major revisions. This value can be changed by the EEPROM to implement an application release number.

### 5.5.5 (Address F3h; MAXPWR) Maximum Power

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:8 | <b>Reserved.</b>  | Yes  | No    | 0             |
| 7:0  | <b>Maximum Power.</b> This register determines the maximum USB power during a 'Get Configuration Descriptor' request. Power is reported in units of 2 mA. | Yes  | Yes   | 0x32          |

## 5.5.6 (Address F4h; USBCTL1) USB Control Register 1

| Bits         | Description   | Read         | Write            | Default Value |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
|--------------|---|--------------|------------------|---------------|---------|-----|---------|-----|---------|-----|---------|-----|----------|---------|----------|-----|----------|-----|----------|-----|-----|---|
| 15:11        | <b>Reserved</b>   | Yes          | No               | 0             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 10:8         | <b>LCLK Frequency.</b> This field determines the frequency of the LCLK output pin<br><table border="0"> <tr> <td><u>Value</u></td> <td><u>Frequency</u></td> </tr> <tr> <td>000</td> <td>0 (off)</td> </tr> <tr> <td>001</td> <td>6 MHz</td> </tr> <tr> <td>010</td> <td>12 MHz</td> </tr> <tr> <td>011</td> <td>24 MHz</td> </tr> <tr> <td>100</td> <td>48 MHz</td> </tr> <tr> <td>101-111</td> <td>Reserved</td> </tr> </table>   | <u>Value</u> | <u>Frequency</u> | 000           | 0 (off) | 001 | 6 MHz   | 010 | 12 MHz  | 011 | 24 MHz  | 100 | 48 MHz   | 101-111 | Reserved | Yes | Yes      | 1   |          |     |     |   |
| <u>Value</u> | <u>Frequency</u>  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 000          | 0 (off)   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 001          | 6 MHz   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 010          | 12 MHz  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 011          | 24 MHz  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 100          | 48 MHz  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 101-111      | Reserved  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 7            | <b>Diagnostic Disconnect.</b> Writing a 1 to this bit causes a single-ended zero to be driven onto the USB for 100 msec, thus simulating a disconnect.  | No           | Yes              | 0             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 6            | <b>Suspend Enable.</b> If clear, the NET1031 does not enter the suspend state. If set, the NET1031 enters the suspend state after detecting 3 msec of inactivity on the USB.  | Yes          | Yes              | 0             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 5            | <b>Wakeup Polarity.</b> If clear, the Wakeup signal is active low. If set, the Wakeup signal is active high.  | Yes          | Yes              | 0             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 4:2          | <b>Wakeup Select.</b> This field selects one of the GIOLINE or GIOPEL inputs to act as a device remote wakeup input.<br><table border="0"> <tr> <td><u>Value</u></td> <td><u>Signal</u></td> </tr> <tr> <td>000</td> <td>GIOPEL0</td> </tr> <tr> <td>001</td> <td>GIOPEL1</td> </tr> <tr> <td>010</td> <td>GIOPEL2</td> </tr> <tr> <td>011</td> <td>GIOPEL3</td> </tr> <tr> <td>100</td> <td>GIOLINE0</td> </tr> <tr> <td>101</td> <td>GIOLINE1</td> </tr> <tr> <td>110</td> <td>GIOLINE2</td> </tr> <tr> <td>111</td> <td>GIOLINE3</td> </tr> </table> | <u>Value</u> | <u>Signal</u>    | 000           | GIOPEL0 | 001 | GIOPEL1 | 010 | GIOPEL2 | 011 | GIOPEL3 | 100 | GIOLINE0 | 101     | GIOLINE1 | 110 | GIOLINE2 | 111 | GIOLINE3 | Yes | Yes | 0 |
| <u>Value</u> | <u>Signal</u>   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 000          | GIOPEL0   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 001          | GIOPEL1   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 010          | GIOPEL2   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 011          | GIOPEL3   |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 100          | GIOLINE0  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 101          | GIOLINE1  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 110          | GIOLINE2  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 111          | GIOLINE3  |              |                  |               |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 1            | <b>Remote Wakeup Support.</b> This field is reported to the Host PC in the USB configuration descriptor's "bmAttributes" field, bit 5, during enumeration, and indicates whether the NET1031 supports device remote wakeup.   | Yes          | Yes              | 1             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |
| 0            | <b>Self-Powered USB Device.</b> This field is reported to the Host PC in the USB configuration descriptor's "bmAttributes" field, bit 6, during enumeration, and indicates if the device is self-powered.   | Yes          | Yes              | 1             |         |     |         |     |         |     |         |     |          |         |          |     |          |     |          |     |     |   |

## 5.5.7 (Address F5h; USBCTL2) USB Control Register 2

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:5 | <b>Reserved</b>  | Yes  | No    | 0             |
| 4    | <b>Language ID String Enable.</b> If set, a language string ID is programmed into the E <sup>2</sup> PROM. The location of the language string is specified by the “ <b>Language String Start Index</b> ” byte in the serial E <sup>2</sup> PROM. If clear, the response to a Language ID String read is determined by the <b>String Default Enable</b> bit.                                 | Yes  | Yes   | 0             |
| 3    | <b>Manufacturer String Enable.</b> If set, a manufacturer’s string is programmed into the E <sup>2</sup> PROM. The location of the manufacturer’s string is specified by the “ <b>Manufacturer String Start Index</b> ” byte in the serial E <sup>2</sup> PROM. If clear, the response to a Manufacturer String read is determined by the <b>String Default Enable</b> bit.                  | Yes  | Yes   | 0             |
| 2    | <b>Product String Enable.</b> If set, a product string is programmed into the E <sup>2</sup> PROM. The location of the product string in the E <sup>2</sup> PROM is specified by the “ <b>Product String Start Index</b> ” byte in the serial E <sup>2</sup> PROM. If clear, the response to a Product String language ID string read is determined by the <b>String Default Enable</b> bit. | Yes  | Yes   | 0             |
| 1    | <b>Serial Number String Enable.</b> If set, a serial number string is programmed into the E <sup>2</sup> PROM. The location of the serial number string is specified by the “ <b>Serial Number String Start Index</b> ” byte in the serial E <sup>2</sup> PROM. If clear, the response to a language ID string read is determined by the <b>String Default Enable</b> bit.                   | Yes  | Yes   | 0             |
| 0    | <b>String Default Enable.</b> If set, default strings are returned to the host if the corresponding String Enable (bits 4:1) is 0. If clear, a string is returned only if the corresponding String Enable (bits 4:1) is 1.   | No   | Yes   | 1             |

## 5.5.8 (Address F6h; STRINDEX1) String Index 1

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:8 | <b>Language ID String Index.</b> This field determines the EEPROM starting word address of the Language ID string.   | Yes  | Yes   | 0             |
| 7:0  | <b>Manufacturer String Index.</b> This field determines the EEPROM starting word address of the Manufacturer string. | Yes  | Yes   | 0             |

## 5.5.9 (Address F7h; STRINDEX2) String Index 2

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:8 | <b>Product String Index.</b> This field determines the EEPROM starting word address of the Product string.             | Yes  | Yes   | 0             |
| 7:0  | <b>Serial Number String Index.</b> This field determines the EEPROM starting word address of the Serial Number string. | Yes  | Yes   | 0             |

## 5.5.10 (Address F8h - FBh; RESERVED) Reserved for future use

## 5.5.11 (Address FCh; EECTL) EEPROM Control

NOTE: These bits should be returned to 0 after being used for an EEPROM access.

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:4 | <b>Reserved.</b>   | Yes  | No    | 0             |
| 3    | <b>REGCEEDO.</b> This bit is used to read the EEPROM read data (EEDO/IDSEL3 pin) when the EEPROM is being accessed from the Host. This bit operates only if the INITSEL pins are not set to 4.     | Yes  | No    | 0             |
| 2    | <b>REGCEEDI.</b> This bit is used to control the EEPROM write data (EEDI/IDSEL2 pin) when the EEPROM is being accessed from the Host. This bit operates only if the INITSEL pins are not set to 4. | Yes  | Yes   | 0             |
| 1    | <b>REGEEKSK.</b> This bit is used to control the EEPROM clock (EESK/IDSEL1 pin) when the EEPROM is being accessed from the Host. This bit operates only if the INITSEL pins are not set to 4.      | Yes  | Yes   | 0             |
| 0    | <b>REGEECS.</b> This bit is used to control the EEPROM chip select (EECS/IDSEL0 pin) when the EEPROM is being accessed from the Host. This bit operates only if the INITSEL pins are not set to 4. | Yes  | Yes   | 0             |

## 5.5.12 (Address FDh; EEADDR) EEPROM Address

| Bits | Description  | Read | Write   | Default Value |
|------|--|------|---------|---------------|
| 15   | <b>EEPROM Start.</b> When this bit is set, a host read or write to a MicroWire EEPROM is initiated. This bit is automatically cleared when the operation completes.                | Yes  | Yes/Set | 0             |
| 14   | <b>EEPROM Read/Write.</b> This bit determines the direction of the host access to the MicroWire EEPROM. If clear, a write access is performed. If set, a read access is performed. | Yes  | Yes     | 0             |
| 13:8 | <b>Reserved.</b>   | Yes  | No      | 0             |
| 7:0  | <b>EEPROM Address.</b> This field selects the word address of EEPROM reads or writes that are initiated by the host.   | Yes  | Yes     | 0             |

## 5.5.13 (Address FEh; EEDATA) EEPROM Data

| Bits | Description   | Read | Write | Default Value |
|------|---|------|-------|---------------|
| 15:0 | <b>EEPROM Data.</b> This register sources data written to the MicroWire EEPROM from the host. At the completion of a host EEPROM read, the data is stored into this register. | Yes  | Yes   | 0             |

## 5.5.14 (Address FFh; REVISION) NET1031 Silicon Revision

| Bits | Description  | Read | Write | Default Value |
|------|--|------|-------|---------------|
| 15:0 | <b>NET1031 Silicon Revision.</b> This is the Silicon Revision Number for the NET1031 | Yes  | No    | RELNUM        |

Note: RELNUM is the silicon revision, encoded as a 4-digit BCD value. The value of RELNUM for the first release of the chip is 0x0100. The least-significant two digits are incremented for mask changes, and the most-significant two digits increment for major revisions. This value cannot be changed.

## 6 USB Vendor-Specific Device Requests (Endpoint 0)

Vendor specific requests to endpoint 0 are used to access the internal registers of the NET1031, as well as I/O devices external to the NET1031. Bit 15 of the wValue field of the setup packet is used to select between register and I/O accesses. It must be low for register accesses and high for I/O accesses. For register accesses, bits 7:0 of the wValue determine the address of the first register. For I/O cycles, the first address is derived from bits 14:0 of the wValue field, and is driven on bits 14:0 of the SRAM address bus. The data passes over the SRAM data bus, SRAMDATA, or the Scan data bus, SCANDATA. A bRequest of 4 is used for all register and I/O accesses.

### 6.1 Register Write

A vendor request to endpoint 0 is used to perform register writes. Either one or two 16-bit writes can be performed for each transfer. The data is not written to the target register until it has been determined that the USB transfer was successful. The target register address is passed in bits 7:0 of the wValue field of the setup packet. If two 16-bit registers are written, the address of the second register is one greater than the value in the wValue field. If the wLength field is not 2 or 4, the endpoint will return a stall acknowledge.

| Setup Byte | Contents      | Description  |
|------------|---------------|--|
| 0          | bmRequestType | Bit 7 = direction (0=Out)<br>Bits 6:5 = type (2=vendor)<br>Bits 4:0 = Recipient (0 = device) |
| 1          | bRequest      | 4 = Register or I/O access   |
| 2          | wValue (LSB)  | Register Address (LSB)   |
| 3          | wValue (MSB)  | Register Address (MSB) (bit 15 = 0)  |
| 4          | wIndex (LSB)  | unused   |
| 5          | wIndex (MSB)  | unused   |
| 6          | wLength (LSB) | Number of bytes to write (LSB), must be 2 or 4   |
| 7          | wLength (MSB) | Number of bytes to write (MSB), must be 0  |

Following is a description of the contents of the OUT packet associated with this control write transfer.

| Byte Index   | Contents                    |
|--------------|-----------------------------|
| 0            | Register Write Data 0 (LSB) |
| 1            | Register Write Data 0 (MSB) |
| 2 (optional) | Register Write Data 1 (LSB) |
| 3 (optional) | Register Write Data 1 (MSB) |



## 6.2 Register Read

A vendor request to endpoint 0 is used to perform register reads. Only one 16-bit read can be performed for each transfer. The target register address is passed in bits 7:0 of the wValue field of the setup packet. If the wLength field is not 2, the endpoint will return a stall acknowledge.

| Setup Byte | Contents      | Description   |
|------------|---------------|---|
| 0          | bmRequestType | Bit 7 = direction (1=IN)<br>Bits 6:5 = type (2=vendor)<br>Bits 4:0 = Recipient (0 = device) |
| 1          | bRequest      | 4 = Register or I/O access  |
| 2          | wValue (LSB)  | Register Address (LSB)  |
| 3          | wValue (MSB)  | Register Address (MSB) (bit 15 = 0)   |
| 4          | wIndex (LSB)  | unused  |
| 5          | wIndex (MSB)  | unused  |
| 6          | wLength (LSB) | Number of bytes to read (LSB), must be 2  |
| 7          | wLength (MSB) | Number of bytes to read (MSB), must be 0  |

Following is a description of the contents of the IN packet associated with this control read transfer.

| Byte Index | Contents                 |
|------------|--------------------------|
| 0          | Register Read Data (LSB) |
| 1          | Register Read Data (MSB) |

## 6.3 I/O Write

A vendor request to endpoint 0 is used to perform I/O writes. Either one or two 16-bit writes can be performed for each transfer. The I/O write cycles are not performed until it has been determined that the USB transfer was successful. The target I/O address is passed in bits 14:0 of the wValue field of the setup packet. If two 16-bit I/O writes occur, the address of the second I/O cycle is one greater than the value in the wValue field. If the wLength field is not 2 or 4, the endpoint will return a stall acknowledge.

| Setup Byte | Contents      | Description  |
|------------|---------------|--|
| 0          | bmRequestType | Bit 7 = direction (0=Out)<br>Bits 6:5 = type (2=vendor)<br>Bits 4:0 = Recipient (0 = device) |
| 1          | bRequest      | 4 = Register or I/O access   |
| 2          | wValue (LSB)  | I/O Address (LSB)  |
| 3          | wValue (MSB)  | I/O Address (MSB) (bit 15 = 1)   |
| 4          | wIndex (LSB)  | unused   |
| 5          | wIndex (MSB)  | unused   |
| 6          | wLength (LSB) | Number of bytes to write (LSB), must be 2 or 4   |
| 7          | wLength (MSB) | Number of bytes to write (MSB), must be 0  |

Following is a description of the contents of the OUT packet associated with this control write transfer.

| Byte Index   | Contents               |
|--------------|------------------------|
| 0            | I/O Write Data 0 (LSB) |
| 1            | I/O Write Data 0 (MSB) |
| 2 (optional) | I/O Write Data 1 (LSB) |
| 3 (optional) | I/O Write Data 1 (MSB) |

## 6.4 I/O Read

A vendor request to endpoint 0 is used to perform I/O reads. Only one 16-bit read can be performed for each transfer. The target I/O address is passed in bits 14:0 of the wValue field of the setup packet. If the wLength field is not 2, the endpoint will return a stall acknowledge.

| Setup Byte | Contents      | Description   |
|------------|---------------|---|
| 0          | bmRequestType | Bit 7 = direction (1=IN)<br>Bits 6:5 = type (2=vendor)<br>Bits 4:0 = Recipient (0 = device) |
| 1          | bRequest      | 4 = Register or I/O access  |
| 2          | wValue (LSB)  | Register Address (LSB)  |
| 3          | wValue (MSB)  | Register Address (MSB) (bit 15 = 1)   |
| 4          | wIndex (LSB)  | unused  |
| 5          | wIndex (MSB)  | unused  |
| 6          | wLength (LSB) | Number of bytes to read (LSB), must be 2  |
| 7          | wLength (MSB) | Number of bytes to read (MSB), must be 0  |

Following is a description of the contents of the IN packet associated with this control read transfer.

| Byte Index | Contents            |
|------------|---------------------|
| 0          | I/O Read Data (LSB) |
| 1          | I/O Read Data (MSB) |

## 6.5 Manufacturer Test Mode

A vendor specific request can be used to set or clear the Timing Test Mode bit.

### 6.5.1 6.5.1 Device Clear Feature (Timing Test Mode)

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Clear the selected device feature<br>wValue = 0x80 --> Timing test mode (clears test bit)<br>wIndex ignored<br>wLength = 0 | --            |

### 6.5.2 6.5.2 Device Set Feature (Timing Test Mode)

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Set the selected device feature<br>wValue = 0x80 --> Timing test mode (sets test bit)<br>wIndex ignored<br>wLength = 0 | --            |

## 7 USB Standard Device Requests (Endpoint 0)

### 7.1 Control 'IN' Transactions

#### 7.1.1 Get Device Status

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| 0      | 2               | bits 15:2 = Reserved<br>bit 1 = Device Remote Wakeup enabled<br>bit 0 = Power supply is good in Self-Powered mode.<br>(depends on PWRGOOD input pin) | 0x0001        |

#### 7.1.2 Get Interface Status

| Offset | Number of Bytes | Description          | Default Value |
|--------|-----------------|----------------------|---------------|
| 0      | 2               | bits 15:0 = Reserved | 0x0000        |

#### 7.1.3 Get Endpoint 0x00, 0x01, 0x81, 0x82 Status

| Offset | Number of Bytes | Description   | Default Value |
|--------|-----------------|---|---------------|
| 0      | 2               | bits 15:1 = Reserved<br>bit 0 = Endpoint is stalled | 0x0000        |

#### 7.1.4 Get Device Descriptor (18 Bytes)

| Offset | Number of Bytes | Description   | Default Value  |
|--------|-----------------|---|--|
| 0      | 1               | Length  | 0x12   |
| 1      | 1               | Type (device)                                       | 0x01   |
| 2      | 2               | USB Specification Release Number                    | 0x0101   |
| 4      | 1               | Class Code  | 0x00   |
| 5      | 1               | Sub Class Code                                      | 0x00   |
| 6      | 1               | Protocol  | 0x00   |
| 7      | 1               | Maximum Endpoint 0 Packet Size                      | 0x08   |
| 8      | 2               | Vendor ID   | Value of <b>VID</b> register   |
| 10     | 2               | Product ID  | Value of <b>PID</b> register   |
| 12     | 2               | Device Release Number                               | Value of <b>RELEASENUM</b> register  |
| 14     | 1               | Index of string descriptor describing manufacturer  | 0x01 (if <b>USBCTL Mfg. String Enable = 1</b> )<br>0x00 (if <b>USBCTL Mfg. String Enable = 0</b> )   |
| 15     | 1               | Index of string descriptor describing product       | 0x02 (if <b>USBCTL Prod. String Enable = 1</b> )<br>0x00 (if <b>USBCTL Prod. String Enable = 0</b> ) |
| 16     | 1               | Index of string descriptor describing serial number | 0x03 (if <b>USBCTL Ser. String Enable = 1</b> )<br>0x00 (if <b>USBCTL Ser. String Enable = 0</b> )   |
| 17     | 1               | Number of configurations                            | 0x01   |

## 7.1.5 Get Configuration Descriptor (39 bytes)

Note that all interface and endpoint descriptors are returned when this request is issued

| Offset                          | Number of Bytes | Description   | Default Value                     |
|---------------------------------|-----------------|---|-----------------------------------|
| <b>Configuration Descriptor</b> |                 |   |                                   |
| 0                               | 1               | Length  | 0x09                              |
| 1                               | 1               | Type (configuration)  | 0x02                              |
| 2                               | 2               | Total length returned for this configuration  | 0x0027                            |
| 4                               | 1               | Number of Interfaces  | 0x01                              |
| 5                               | 1               | Number of this configuration  | 0x01                              |
| 6                               | 1               | Index of string descriptor describing this configuration  | 0x00                              |
| 7                               | 1               | Attributes<br>bit 7 = 1<br>bit 6 = Self-Powered (based on "Self-Power" <b>USBCTL</b> register field)<br>bit 5 = Remote Wakeup capability (based on "Remote-Wakeup Support" <b>USBCTL</b> register field)<br>bits 4:0 = Reserved | 0xE0                              |
| 8                               | 1               | Maximum USB power required (in 2 mA units)  | Value in <b>MAXPOWER</b> register |
| <b>Interface 0 Descriptor</b>   |                 |   |                                   |
| 0                               | 1               | Size of this descriptor in bytes  | 0x09                              |
| 1                               | 1               | Type (interface)  | 0x04                              |
| 2                               | 1               | Number of this interface  | 0x00                              |
| 3                               | 1               | Alternate Interface   | 0x00                              |
| 4                               | 1               | Number of endpoints used by this interface (excluding endpoint 0)   | 0x03                              |
| 5                               | 1               | Class Code  | 0xFF                              |
| 6                               | 1               | Sub Class Code  | 0x00                              |
| 7                               | 1               | Device Protocol   | 0x00                              |
| 8                               | 1               | Index of string descriptor describing this interface  | 0x00                              |
| <b>Endpoint 1 Descriptor</b>    |                 |   |                                   |
| 0                               | 1               | Size of this descriptor   | 0x07                              |
| 1                               | 1               | Descriptor Type (endpoint)  | 0x05                              |
| 2                               | 1               | Endpoint Address<br>bit 7 = direction (1 = IN, 0 = OUT)<br>bits 6:4 = reserved<br>bits 3:0 = endpoint number  | 0x01                              |
| 3                               | 1               | Endpoint Attributes<br>bits 7:2 = reserved<br>bits 1:0<br>00 = Control<br>01 = Isochronous<br>10 = Bulk<br>11 = Interrupt   | 0x02                              |
| 4                               | 2               | Maximum packet size of this endpoint  | 0x0040                            |
| 6                               | 1               | Interval for polling endpoint (not used)  | 0x00                              |

## Get Configuration Descriptor (continued)

| Offset                          | Number of Bytes | Description   | Default Value |
|---------------------------------|-----------------|---|---------------|
| <b>Endpoint 0x81 Descriptor</b> |                 |   |               |
| 0                               | 1               | Size of this descriptor   | 0x07          |
| 1                               | 1               | Descriptor Type (endpoint)  | 0x05          |
| 2                               | 1               | Endpoint Address<br>bit 7 = direction (1 = IN, 0 = OUT)<br>bits 6:4 = reserved<br>bits 3:0 = endpoint number              | 0x81          |
| 3                               | 1               | Endpoint Attributes<br>bits 7:2 = reserved<br>bits 1:0<br>00 = Control<br>01 = Isochronous<br>10 = Bulk<br>11 = Interrupt | 0x02          |
| 4                               | 2               | Maximum packet size of this endpoint  | 0x0040        |
| 6                               | 1               | Interval for polling endpoint (in ms)   | 0x00          |
| <b>Endpoint 0x82 Descriptor</b> |                 |   |               |
| 0                               | 1               | Size of this descriptor   | 0x07          |
| 1                               | 1               | Descriptor Type (endpoint)  | 0x05          |
| 2                               | 1               | Endpoint Address<br>bit 7 = direction (1 = IN, 0 = OUT)<br>bits 6:4 = reserved<br>bits 3:0 = endpoint number              | 0x82          |
| 3                               | 1               | Endpoint Attributes<br>bits 7:2 = reserved<br>bits 1:0<br>00 = Control<br>01 = Isochronous<br>10 = Bulk<br>11 = Interrupt | 0x03          |
| 4                               | 2               | Maximum packet size of this endpoint  | 0x0004        |
| 6                               | 1               | Interval for polling endpoint (in ms)   | 0x40          |

## 7.1.6 Get String Descriptor 0

| Offset | Number of Bytes | Description                           | Default Value        |
|--------|-----------------|---------------------------------------|----------------------|
| 0      | 4               | Language ID (English = 09, U.S. = 04) | 0x04, 0x03<br>0x0409 |

## 7.1.7 Get String Descriptor 1

| Offset | Number of Bytes | Description             | Default Value                         |
|--------|-----------------|-------------------------|---------------------------------------|
| 0      | 38              | Manufacturer Descriptor | 0x26, 0x03<br>"Netchip<br>Technology" |

## Get Configuration Descriptor (continued)

## 7.1.8 Get String Descriptor 2

| Offset | Number of Bytes | Description        | Default Value                                     |
|--------|-----------------|--------------------|---|
| 0      | 62              | Product Descriptor | 0x3E, 0x03<br>"NET1031 USB<br>Scanner Controller" |

## 7.1.9 Get String Descriptor 3

| Offset | Number of Bytes | Description              | Default Value        |
|--------|-----------------|--------------------------|----------------------|
| 0      | 10              | Serial Number Descriptor | 0x0A, 0x03<br>"1001" |

## 7.1.10 Get Configuration

| Offset | Number of Bytes | Description                          | Default Value |
|--------|-----------------|--------------------------------------|---------------|
| 0      | 1               | Returns current device configuration | 0x00          |

## 7.1.11 Get Interface

| Offset | Number of Bytes | Description   | Default Value |
|--------|-----------------|---|---------------|
| 0      | 1               | Returns current alternate setting for the specified interface | 0x0           |

## 7.2 Control 'OUT' Transactions

### 7.2.1 Set Address

| Offset | Number of Bytes | Description   | Default Value |
|--------|-----------------|---|---------------|
| --     | 0               | Sets USB address of device<br>Value = device address, Index = 0 | --            |

### 7.2.2 Set Configuration

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Sets the device configuration<br>Value = Configuration value (0 or 1 supported), | --            |

### 7.2.3 Set Interface

| Offset | Number of Bytes | Description   | Default Value |
|--------|-----------------|---|---------------|
| --     | 0               | Selects alternate setting for specified interface<br>Value = Alternate setting, Index = specified interface | --            |

### 7.2.4 Device Clear Feature

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Clear the selected device feature<br>Value = feature selector<br>FS = 1 --> Device Remote Wakeup (disable) | --            |

### 7.2.5 Device Set Feature

| Offset | Number of Bytes | Description   | Default Value |
|--------|-----------------|---|---------------|
| --     | 0               | Set the selected device feature<br>Value = feature selector<br>FS = 1 --> Device Remote Wakeup (enable) | --            |

### 7.2.6 Endpoint Clear Feature

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Clear the selected endpoint feature<br>Value = feature selector, Index = endpoint number<br>FS = 0 --> Endpoint stall (clears stall bit) | --            |

### 7.2.7 Endpoint Set Feature

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 0               | Set the selected endpoint feature<br>Value = feature selector, Index = endpoint number<br>FS = 0 --> Endpoint stall (sets stall bit) | --            |

## 8 Bulk and Interrupt Endpoints

### 8.1 Endpoint 0x01 'OUT' Transactions (SRAM Write Pipe)

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | up to 64        | Host writes data to the external SRAM using bulk OUT transactions. | --            |

### 8.2 Endpoint 0x81 'IN' Transactions (SRAM/Image Data Read Pipe)

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 64              | Host reads data from the external SRAM or image data from the SRAM transmit FIFO using bulk IN transactions. | --            |

### 8.3 Endpoint 0x82 'IN' Transactions (Status Input Pipe)

| Offset | Number of Bytes | Description  | Default Value |
|--------|-----------------|--|---------------|
| --     | 4               | Host reads 4 bytes of status information from this endpoint using an interrupt IN transaction. | --            |

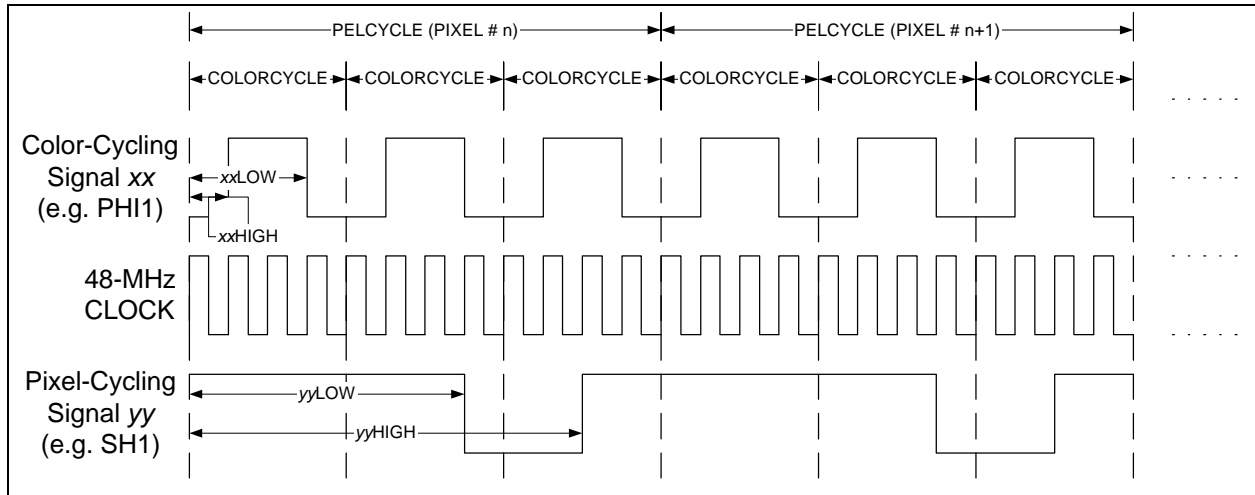


## 9 Signal Timing

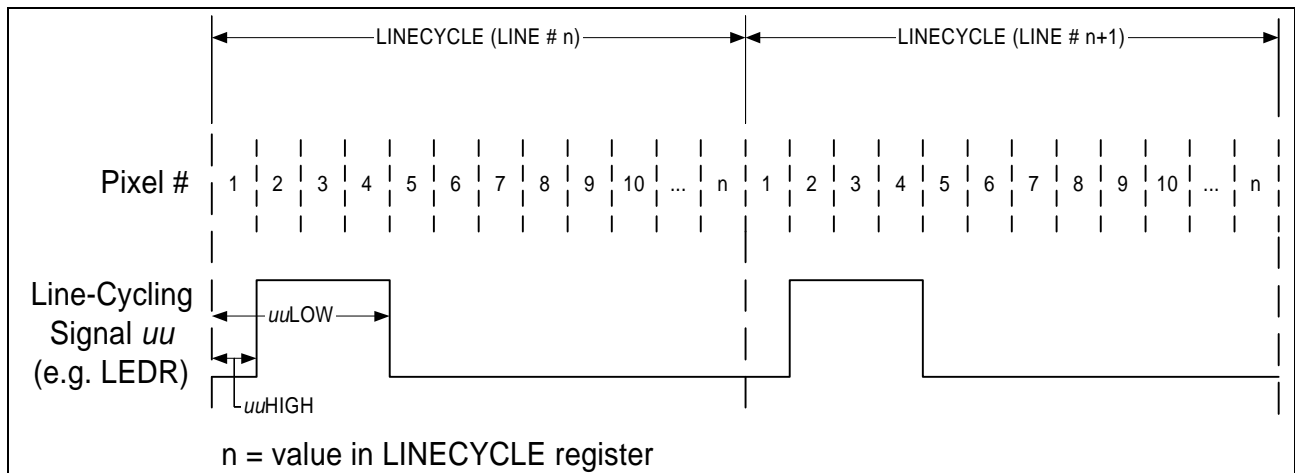
### 9.1 Signal Timing

Pulse Width Modulated (PWM) signals are defined by the PWM registers. Each PWM signal has three associated registers: *xxxxCTL*, *xxxxHIGH*, and *xxxxLOW*. Additionally, some PWM registers are based on a color or pixel cycle, some are based on a line cycle, and some are based on a stepper cycle. The *xxx* is replaced by the signal name for each register. The following figures show how these parameters affect the timing of a PWM signal.

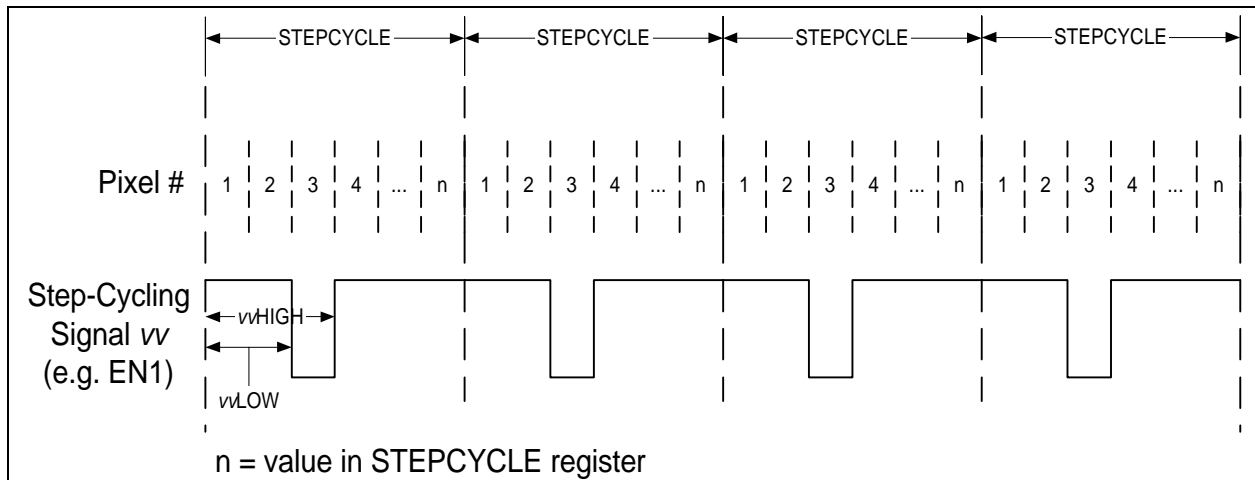
#### 9.1.1 Color- and Pixel-Based Signal Timing



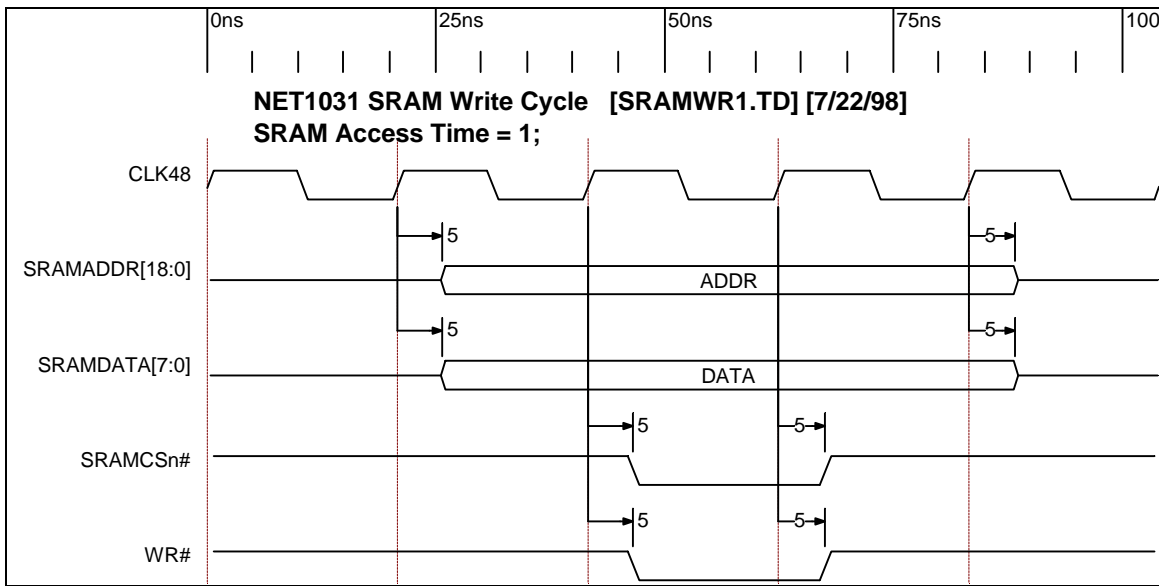
#### 9.1.2 Line-Based Signal Timing



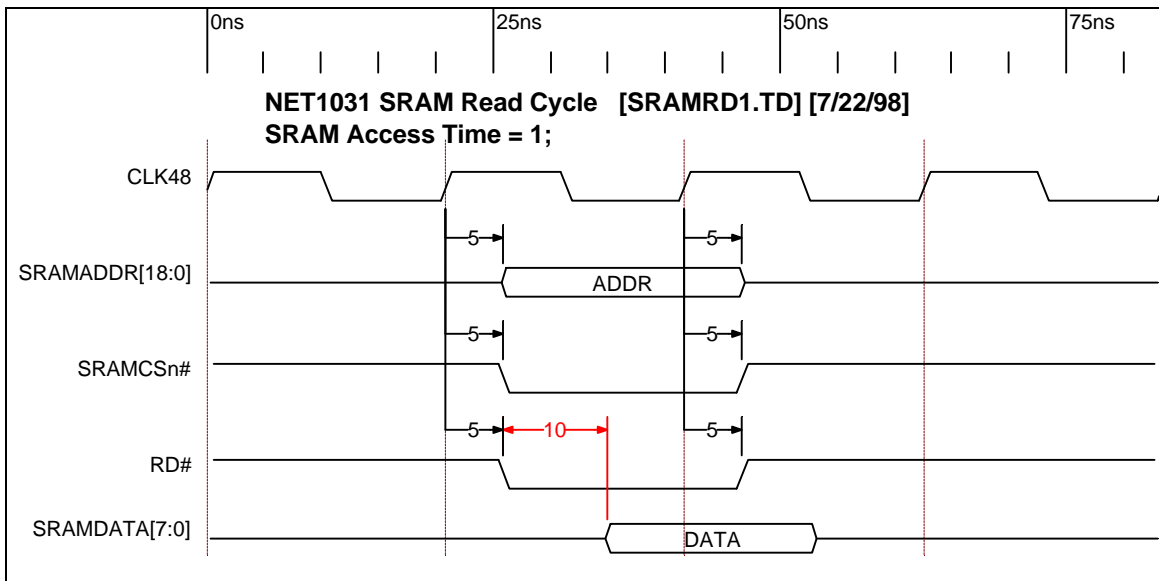
9.1.3 Stepper-Based Signal Timing



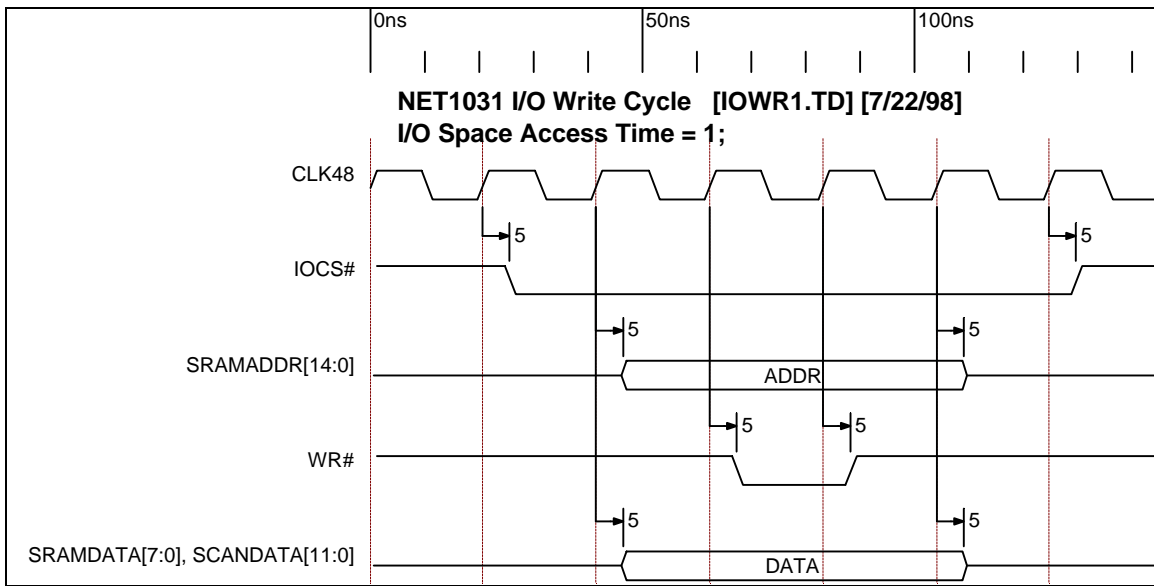
### 9.2 SRAM Write Timing



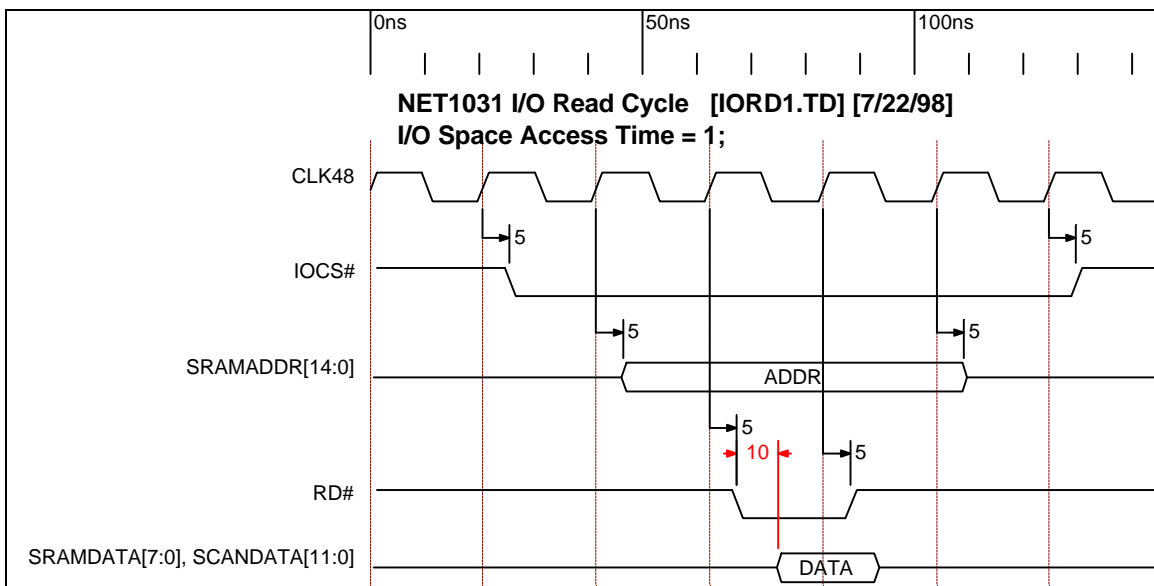
### 9.3 SRAM Read Timing



### 9.4 I/O Write Timing



### 9.5 I/O Read Timing



## 10 Electrical Specifications

### 10.1 Absolute Maximum Ratings

Conditions that exceed the Absolute Maximum limits may destroy the device.

| Symbol             | Parameter                  | Conditions             | Min  | Max                  | Unit |
|--------------------|----------------------------|------------------------|------|----------------------|------|
| V <sub>DDC</sub>   | Core/USB Supply Voltage    | With Respect to Ground | -0.5 | 4.6                  | V    |
| V <sub>DDLCL</sub> | Local Supply Voltage (+5V) | With Respect to Ground | -0.5 | 7.0                  | V    |
| V <sub>I</sub>     | DC input voltage           | With Respect to Ground | -0.5 | V <sub>DD</sub> +0.5 | V    |
| I <sub>OUT</sub>   | DC Output Current, per pin |                        | -25  | 25                   | mA   |
| T <sub>STG</sub>   | Storage Temperature        | No bias                | -65  | 150                  | °C   |
| T <sub>AMB</sub>   | Ambient temperature        | Under bias             |      |                      | °C   |
| T <sub>J</sub>     | Junction temperature       | Under bias             |      |                      | °C   |
| P <sub>D</sub>     | Power Dissipation          | Under bias             |      |                      | mW   |
| V <sub>ESD</sub>   | ESD Rating                 | R = 1.5K, C = 100pF    |      | 2                    | KV   |

### 10.2 Recommended Operating Conditions

Conditions that exceed the Operating limits may cause the device to function incorrectly.

| Symbol             | Parameter                | Conditions     | Min  | Max              | Unit |
|--------------------|--------------------------|----------------|------|------------------|------|
| V <sub>DDC</sub>   | Core/USB Supply Voltage  |                | 3.0  | 3.6              | V    |
| V <sub>DDLCL</sub> | Local Bus Supply Voltage | 5.0V operation | 4.75 | 5.25             | V    |
| V <sub>DDLCL</sub> | Local Bus Supply Voltage | 3.3V operation | 3.0  | 3.6              | V    |
| V <sub>IH</sub>    | High Level Input Voltage |                | 2    |                  | V    |
| V <sub>IL</sub>    | Low Level Input Voltage  |                |      | 0.8              | V    |
| V <sub>I</sub>     | Input Voltage            |                | 0    | V <sub>DDL</sub> | V    |
| V <sub>O</sub>     | Output Voltage           |                | 0    | V <sub>DDL</sub> | V    |
|                    |                          |                |      |                  |      |
| T <sub>A</sub>     | Operating Temperature    |                | 0    | 70               | °C   |
| t <sub>R</sub>     | Input rise time          |                | 1    | 10               | ns/V |
| t <sub>F</sub>     | Input fall time          |                | 1    | 10               | ns/V |

### 10.3 DC Specifications

#### 10.3.1 Core DC Specifications

Operating Conditions: V<sub>DDC</sub>: 3.3V ± 5%, T<sub>A</sub> = 0°C to 70°C

All typical values are at V<sub>DDC</sub> = 3.3V and T<sub>A</sub> = 25°C

Operating Conditions: Notes 1, 2, 9.

| Symbol            | Parameter                                 | Conditions              | Min | Typ | Max | Unit |
|-------------------|---|-------------------------|-----|-----|-----|------|
| I <sub>DDC</sub>  | V <sub>DDC</sub> Supply Current           | V <sub>DDC</sub> = 3.3V |     | 100 | 170 | mA   |
| I <sub>DDCS</sub> | V <sub>DDC</sub> Supply Current (Suspend) | Device suspended        |     |     | 220 | μA   |

### 10.3.2 USB Port DC Specifications

Operating Conditions:  $V_{DDC} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

All typical values are at  $V_{DDC} = 3.3V$  and  $T_A = 25^\circ C$

Operating Conditions: Notes 1,2.

| Symbol   | Parameter                       | Conditions                      | Min | Typ | Max | Unit    |
|----------|---------------------------------|---------------------------------|-----|-----|-----|---------|
| $V_{DI}$ | Differential Input Sensitivity  | $ (D+) - (D-) $                 | 0.2 |     |     | V       |
| $V_{CM}$ | Differential Common Mode Range  | Includes VDI range              | 0.8 |     | 2.5 | V       |
| $V_{SE}$ | Single Ended Receiver Threshold |                                 | 0.8 |     | 2.0 | V       |
| $V_{OH}$ | Static Output High              | $R_L$ of 15 K $\Omega$ to GND   | 2.8 |     | 3.6 | V       |
| $V_{OL}$ | Static Output Low               | $R_L$ of 1.5 K $\Omega$ to 3.6V |     |     | 0.3 | V       |
| $I_{LO}$ | Hi-Z State Data Line Leakage    | $0V < V_{IN} < 3.3V$            | -10 |     | +10 | $\mu A$ |
| $C_{IO}$ | I/O Capacitance                 | Pin to GND                      |     |     | 20  | pF      |

### 10.3.3 Local Bus (+3.3V) DC Specifications

Operating Conditions:  $V_{DDL} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

All typical values are at  $V_{DDL} = 3.3V$  and  $T_A = 25^\circ C$

Operating Conditions: Note 9

| Symbol     | Parameter                          | Conditions                           | Min         | Typ | Max | Unit    |
|------------|------------------------------------|--------------------------------------|-------------|-----|-----|---------|
| $V_{OH}$   | Output High Voltage                | $I_{OH1} = -6mA$ , $I_{OH2} = -12mA$ | VDD<br>-0.4 |     |     | V       |
| $V_{OL}$   | Output Low Voltage                 | $I_{OL1} = 6mA$ , $I_{OL2} = 12mA$   |             |     | 0.4 | V       |
| $I_{IH}$   | Input High Leakage                 | $V_{IH} = 3.3V$                      | -1          |     | 1   | $\mu A$ |
| $I_{IL}$   | Input Low Leakage                  | $V_{IL} = 0V$                        | -1          |     | 1   | $\mu A$ |
| $I_{OZ}$   | Hi-Z State Data Line Leakage       | $0V < V_{IN} < 3.3V$                 | -1          |     | 1   | $\mu A$ |
| $I_{DDLS}$ | $V_{DDL}$ Supply Current (Suspend) | Device suspended                     |             |     | 80  | $\mu A$ |
| $I_{DDL}$  | $V_{DDL}$ Supply Current           | $V_{DDC} = 3.3V$                     |             | 50  | 70  | mA      |
| $C_{IO}$   | I/O Capacitance                    | Pin to GND                           |             |     | 10  | pF      |
| $C_{IN}$   | Input Capacitance                  | Pin to GND                           |             |     | 10  | pF      |

## 10.3.4 Local Bus (+5.0V) DC Specifications

Operating Conditions:  $V_{DDL} = 5.0V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ All typical values are at  $V_{DDL} = 5.0V$  and  $T_A = 25^\circ C$ 

Operating Conditions: Note 9

| Symbol     | Parameter                          | Conditions                          | Min            | Typ | Max | Unit    |
|------------|------------------------------------|-------------------------------------|----------------|-----|-----|---------|
| $V_{OH}$   | Output High Voltage                | $I_{OH1} = -3mA$ , $I_{OH2} = -6mA$ | $V_{DD} - 0.4$ |     |     | V       |
| $V_{OL}$   | Output Low Voltage                 | $I_{OL1} = 6mA$ , $I_{OL2} = 12mA$  |                |     | 0.4 | V       |
| $I_{IH}$   | Input High Leakage                 | $V_{IH} = 5.0V$                     | -1             |     | 1   | $\mu A$ |
| $I_{IL}$   | Input Low Leakage                  | $V_{IL} = 0V$                       | -1             |     | 1   | $\mu A$ |
| $I_{OZ}$   | Hi-Z State Data Line Leakage       | $0V < V_{IN} < 5.0V$                | -1             |     | 1   | $\mu A$ |
| $I_{DDLS}$ | $V_{DDL}$ Supply Current (Suspend) | Device suspended                    |                |     | 100 | $\mu A$ |
| $I_{DDL}$  | $V_{DDL}$ Supply Current           | $V_{DDC} = 3.3V$                    |                | 60  | 80  | mA      |
| $C_{IO}$   | I/O Capacitance                    | Pin to GND                          |                |     | 10  | pF      |
| $C_{IN}$   | Input Capacitance                  | Pin to GND                          |                |     | 10  | pF      |

## 10.4 AC Specifications

### 10.4.1 USB Port AC Specifications

Operating Conditions:  $V_{DD}$ :  $3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$

All typical values are at  $V_{DD} = 3.3V$  and  $T_A = 25^\circ C$

Operating Conditions: Notes 1,2,3.

| Symbol      | Parameter  | Conditions                 | Waveform   | Min   | Typ | Max   | Unit     |
|-------------|--|----------------------------|------------|-------|-----|-------|----------|
| $T_R$       | Rise & Fall Times  | $C_L = 50$ pF<br>Notes 4,5 | Figure 8-1 | 4     |     | 20    | ns       |
| $T_F$       |  |                            |            | 4     |     | 20    |          |
| $T_{RFM}$   | Rise/Fall time matching                                  | $(T_R / T_F)$              | Figure 8-1 | 90    |     | 110   | %        |
| $V_{CRS}$   | Output Signal Crossover Voltage                          |                            |            | 1.3   |     | 2.0   | V        |
| $Z_{DRV}$   | Driver Output Resistance                                 | Steady State Drive         |            | 28    |     | 43    | $\Omega$ |
| $T_{DRATE}$ | Data Rate  |                            |            | 11.97 | 12  | 12.03 | Mbs      |
| $T_{DDJ1}$  | Source Differential Driver Jitter to Next Transition     | Notes 6,7.                 | Figure 8-2 | -3.5  | 0   | 3.5   | ns       |
| $T_{DDJ2}$  | Source Differential Driver Jitter for Paired Transitions | Notes 6,7                  | Figure 8-2 | -4.0  | 0   | 4.0   | ns       |
| $T_{DEOP}$  | Differential to EOP Transition Skew                      | Note 7                     | Figure 8-3 | -2    | 0   | 5     | ns       |
| $T_{EOPT}$  | Source EOP Width   | Note 7                     | Figure 8-3 | 160   | 167 | 175   | ns       |
| $T_{JR1}$   | Receiver Data Jitter Tolerance to Next Transition        | Note 7                     | Figure 8-4 | -18.5 | 0   | 18.5  | ns       |
| $T_{JR2}$   | Receiver Data Jitter Tolerance for Paired Transitions    | Note 7                     | Figure 8-4 | -9    | 0   | 9     | ns       |
| $T_{EOPR1}$ | EOP Width at Receiver; Must reject as EOP                | Note 7                     | Figure 8-3 | 40    |     |       | ns       |
| $T_{EOPR2}$ | EOP Width at Receiver; Must accept as EOP                | Note 7                     | Figure 8-3 | 80    |     |       | ns       |

### 10.4.2 USB Port AC/DC Specification Notes

1. All voltages measured from the local ground potential, unless otherwise specified.
2. All timings use a capacitive load ( $C_L$ ) to ground of 50 pF, unless otherwise specified.
3. Full Speed timings have a 1.5 k $\Omega$  pull-up to 3.3 V on the D+ data line.
4. Measured from 10% to 90% of the data signal.
5. The rising and falling edges should be smoothly transitioning (monotonic).
6. Timing difference between the differential data signals.
7. Measured at crossover point of differential data signals.
8. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub  $V_{BUS}$  droop of 330 mV.
9.  $V_{DDC}$  and  $I_{DDC}$  refer to core power supply (pins designated  $V_{DD}$ ).  $V_{DDL}$  and  $I_{DDL}$  refer to local bus power supply (pins designated  $V_{DD, LOCAL}$ ).



10.4.3 USB Port AC Waveforms

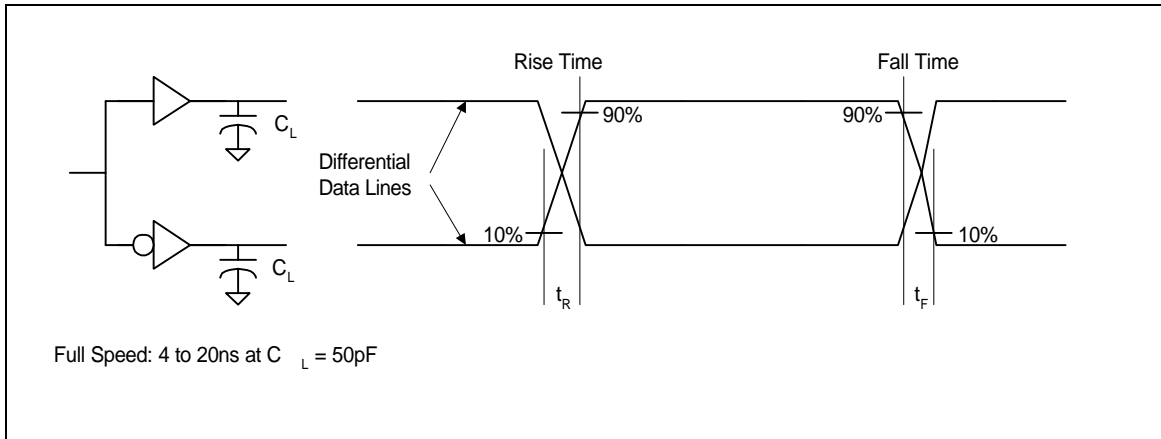


Figure 9-1. Data Signal Rise and Fall Time

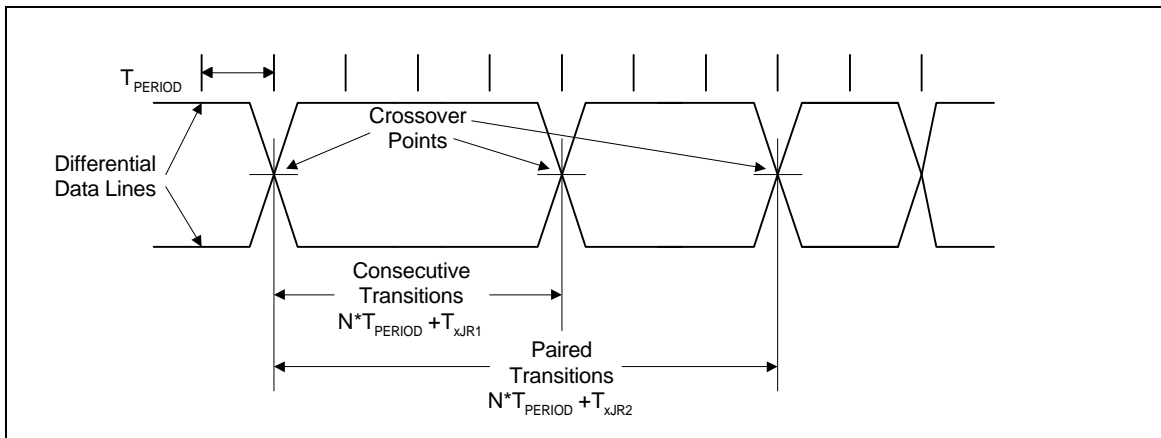
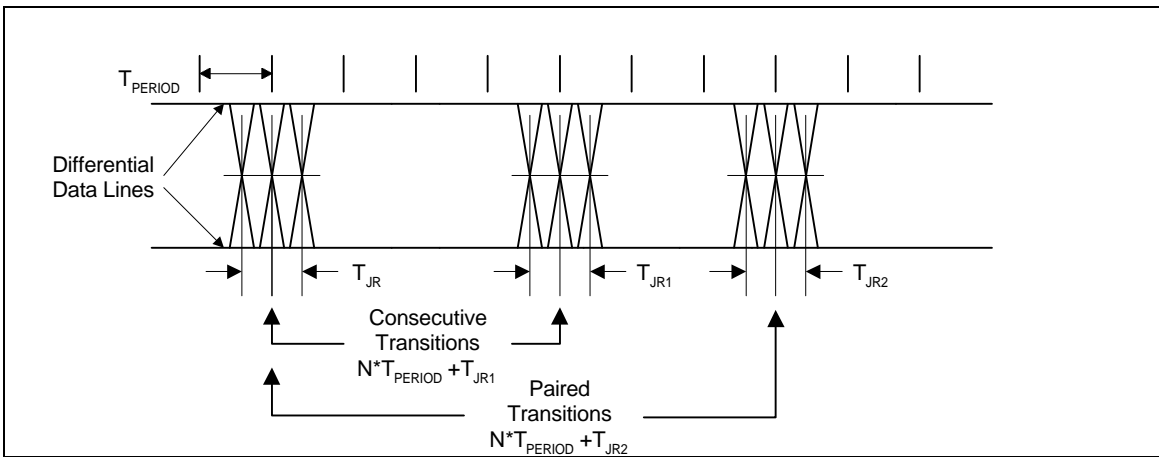
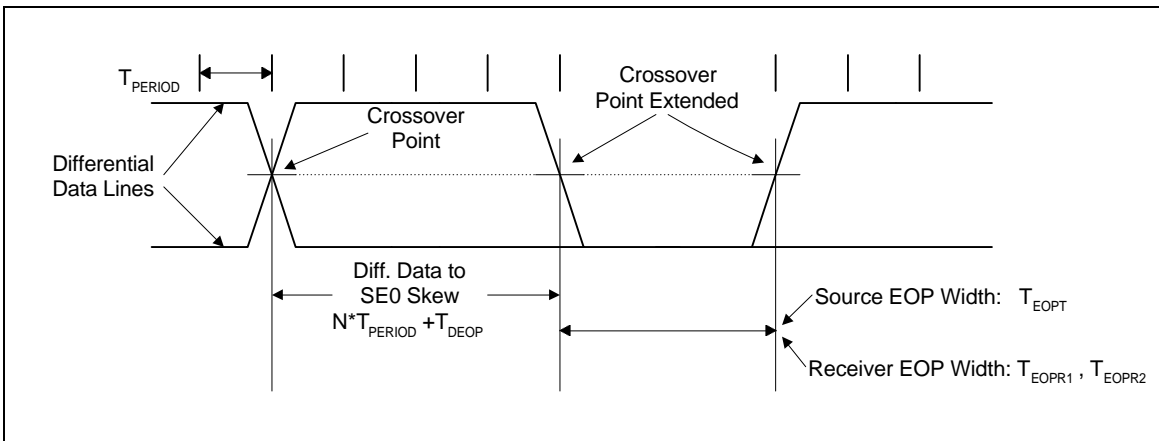


Figure 9-2. Differential Data Jitter



# 11 Mechanical Drawing

Plastic QFP 144pin Body size 28 x 28 x 3.35mm

